ROBO-8120VG2R

Single Host Board

User's Manual

Version 1.0

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Table of Contents

How to Use This Manual

Chapter 1 System Overview 1-1

1.1 Introduction 1-1
1.2 Check List 1-2
1.3 Product Specification 1-2
System Configuration 1-4
1.3.1 Mechanical Drawing 1-6
1.4 System Architecture 1-7

Chapter 2 Hardware Configuration 2-1

2.1 Jumper Setting 2-1
2.2 Connector Allocation 2-4

Chapter 3 System Installation 3-1

3.1 Intel® LGA 1366 Processor 3-1
3.2 Main Memory 3-4
3.3 Installing the Single Board Computer 3-5
3.3.1 Chipset Component Driver 3-5
3.3.2 Intel Integrated Graphics GMCH Chip 3-5
3.3.3 On-board Fast Ethernet Controllers 3-5
3.3.4 On-board High Definition Audio Controller 3-6
3.3.5 Intel Matrix Storage Manager Device 3-6
3.4 Clear CMOS Operation 3-7
3.5 WDT Function 3-8
3.6 GPIO 3-9
3.6.1 Pin assignment 3-9
3.6.2 ROBO-8120VG2R GPIO Programming Guide 3-10

Chapter 4 BIOS Setup Information 4-1

4.1 Entering Setup -- Launch System Setup 4-1
4.2 Main 4-2
4.3 Advanced 4-3
4.4 Chipset 4-16
4.5 Boot 4-24
4.6 Security 4-26
4.7 Save & Exit 4-27
4.8 Event Logs 4-28

Chapter 5 Troubleshooting 5-1

5.1 Hardware Quick Installation 5-1
5.2 BIOS Setting 5-2
5.3 FAQ 5-3

Appendix A

Appendix B

How to Use This Manual

The manual describes how to configure your ROBO-8120VG2R system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides various useful tips to quickly get ROBO-8120VG2R running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site : http://www.portwell.com.tw/.

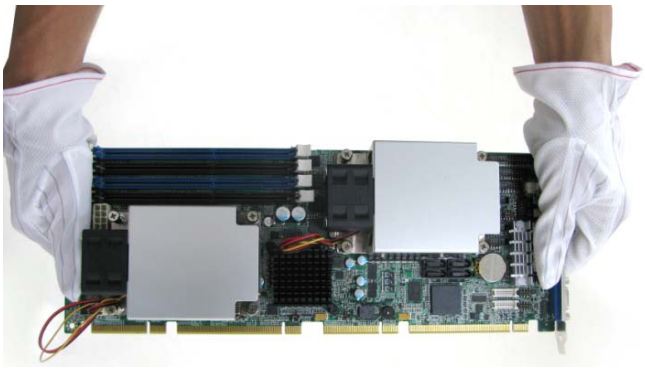
Notice

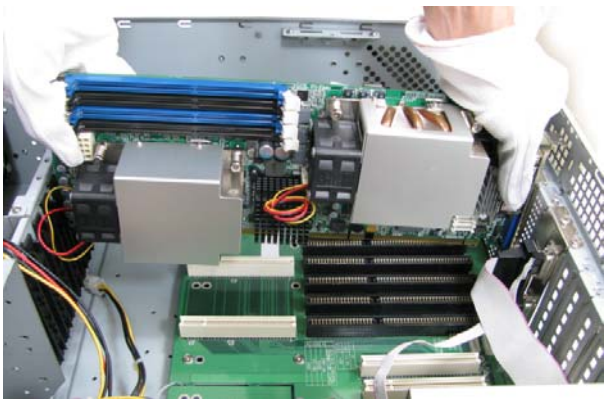
SBC Handling and Installation Notice

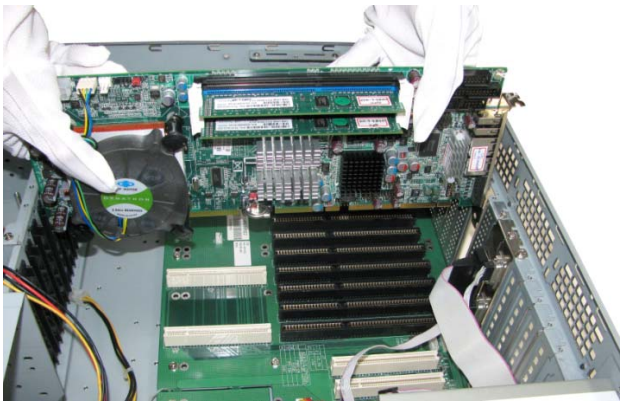
- Handling and Installing SBC

Caution: Do not just hold any single side of the SBC; hold evenly on both sides!

- Heavy processor cooler may bend the SBC when SBC being held just on one side.
- The bending may cause soldering or components damaged.







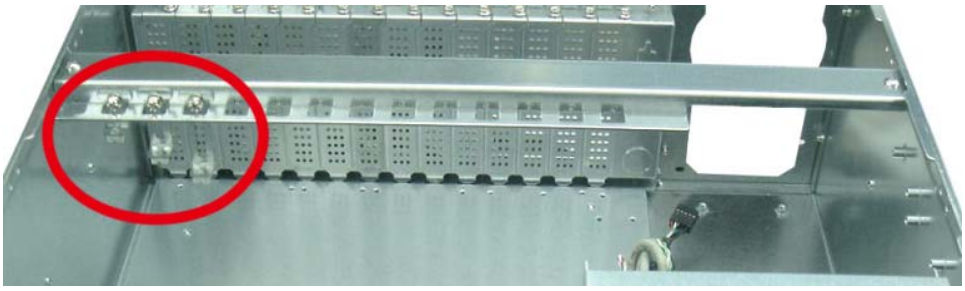
■ Fix your SBC in System

Caution : Suggest your S.I or vendor to use a metal bracket to hold/fix the desktop or server grade SBC to avoid the vibration damage during transportation. Heavy processor cooler may bend the SBC when systems are during transportation without any holder.

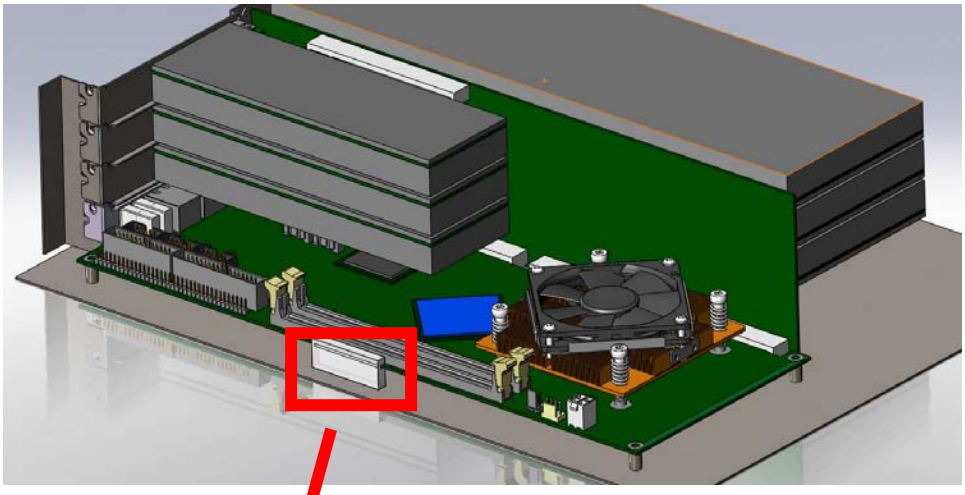
Example:

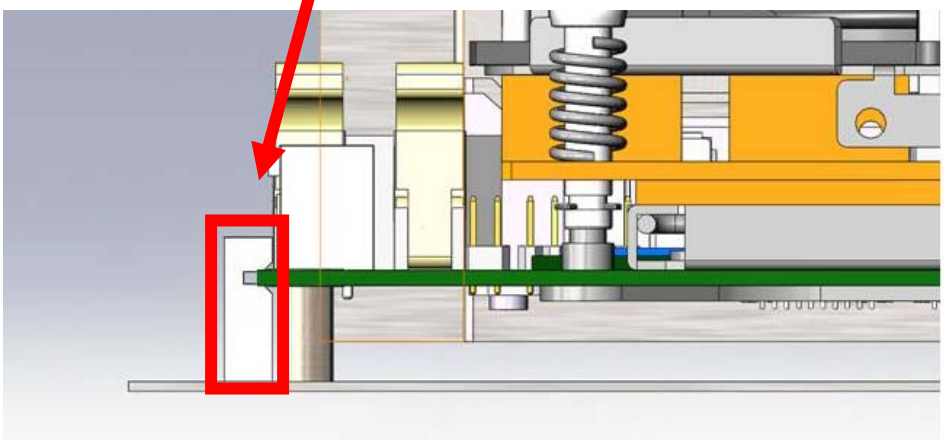
- 4U chassis :

  ➔ Use L type mental or plastic or rubber bracket to hold SBC.



- 2U or 1U chassis: a mental bracket on the bottom of chassis to balance and support SBC from bending.





Chapter 1
System Overview

1.1 Introduction

ROBO-8120VG2R, the PICMG 1.3 Single Host Board supports Intel® high-performance single or dual Dual-Core™/Quad-Core™ Xeon® C5500/C3500 series processors in LGA1366 package which adopts Intel® 3420 chipset. The special design CPU cooler can support single processor up to 85W max. TDP for high computing power and also provide smart fan function support. The board equipped four DDR3 DIMM sockets allows up to 32GB, ECC registered memory for those market segments that could benefit from it such as Medical, data storage, Security, wireless infrastructure and Converged Communications application.

The Intel® C5500/C3500 series processors feature flexible design of dual PCI Express x8 that could be aggregated to one PCI Express x 16 for add-in Graphic cards. It means ROBO-8120VG2R can be suitable for all Portwell's PICMG 1.3 server and non-server grade backplanes for more expansions, and the backplanes support PCI-X slots via PCIe to PCI-X Bridge, Intel® PXH 6700, to improve the bandwidth. And there is one more PCIe x16 links comes from 2nd processor via high-speed signal connector on back side. Via one daughter card, it can route the 2nd PCIex16 to dedicated backplane. The two PCI Express x1 Links are dedicated to Intel® 82574L Gigabit Ethernet controller with two ports which are designed for high performance and low memory latency.

Graphics display is another advantage of this superior SHB because many industries need more than a display of most servers because those applications are image related. ROBO-8120VG2R equipped XGI Z11 graphics processor with PCI Express x1 architecture. Default configuration with 32MB DDR2 video memory delivers solid 2D performance. Optional supports 2nd VGA or DVI-D (TMDS signal) output. ROBO-8120VG2R also provides six Serial ATA 300 ports which supports RAID 0, 1, 5, 10 functions.

ROBO-8120VG2R main features:

- Support Intel® Dual-Core™/Quad-Core™ Xeon® C5500/C3500 series processors in an LGA1366 socket
- Four 240-pin DDR3 SDRAM DIMM socket for two channel, and support for DDR3 1333/1066/800 DIMMs, up to 32GB system memory
- On-Board relative high performance graphic engine, XGI Z11 provides 2D Accelerator with 32MB DDR2 video memory
- Flexible design of dual PCI Express x8 can be aggregated as one PCI Express x16 for the most add-in graphic cards, one PCI Express x 4 link (can be configured as four PCI Express x 1 link), four PCI devices via backplane
- Equipped two Intel® 82574L Gigabit Ethernet controller with dual RJ45 ports
- Rich and powerful I/O that supports six SATA 300 ports, twelve USB 2.0 ports, two serial ports, one parallel port and one FDD channel

1.2 Check List

The ROBO-8120VG2R package should cover the following basic items:

- ✓ One ROBO-8120VG2R Single Host Board
- ✓ One cooler for single CPU
- ✓ One Serial port & Printer port cable kit (2.0mm pitch)
- ✓ One FDD cable
- ✓ Two SATA signal cables
- ✓ One PICMG SBC Handling and Installation Notice
- ✓ One Installation Resources CD-Title

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main processor**
  - Single or Dual Intel® Dual Core™/Quad Core™ Xeon® C5500/C3500 series processor in LGA1366 package

- **BIOS**
  AMI EFI system BIOS with 64MB SPI Flash ROM

- **Main Memory**

  - Support dual-channel & signal channel DDR3 memory interface

  - ECC, registered only

  - Four DIMM sockets support DDR3 1333/1066/800 SDRAM up to 32GB System Memory

- **L2 Cache Memory**
  Built-in Processor

- **Chipset**
  Intel® 3420 chipset

- **Bus Interface**
  Follow PICMG 1.3 RC1.0 standard

- **Floppy Drive Interface**
  Support one FDD port up to two floppy drives and 5-1/4"(360K, 1.2MB), 3-1/2" (720K, 1.2MB, 1.44MB, 2.88MB) diskette format and 3-mode FDD

- **Serial Ports**
  Support one RS232 and one RS232/422/485 selectable

- **Parallel Port**
  Support one parallel port with SPP, EPP and ECP modes

- **USB Interface**
  Support twelve USB (Universal Serial Bus) ports for high-speed I/O peripheral devices (Dual USB ports on bracket, Four USB ports route to backplane.)

- **PS/2 Mouse and Keyboard Interface**
  Support one 2x5-pin connector for PS/2 keyboard/mouse connection

- **Auxiliary I/O Interfaces**
  Keyboard lock and HDD active LED

- **Real Time Clock/Calendar (RTC)**
  Support Y2K Real Time Clock/Calendar with battery backup for 7-year data retention

- **On-board VGA**
  - Via PCI Express x1 bus interface, XGI Z11 graphics processor with 32MB DDR2 memory features high performance 2D Accelerator, high efficient BroadBahn Memory architecture, and high performance Flat Panel Display.
  - One VGA port on bracket
  - Optional support TMDS interface for DVI-D display or second VGA display

- **On-board Ethernet LAN**
  Two PCI Express x1 interface based Intel® 82574L Ethernet controller to support dual Gigabit Ethernet MAC & PHY

- **Expansion Interface**
  Support three PCI Express x4, two PCI Express x8 (or one PCIEx16) links from processors, four PCIe x1 (or one PCIe x4) from chipset, and four PCI devices

- **Cooling Fans**
  Support three 3-pin headers for CPU, and System fans

- **System Monitoring Feature**
  Monitor CPU temperature, system temperature and major power sources, etc

- **Bracket**
  Support dual Ethernet port with 2 indicators, dual USB ports, and one CRT port

- **Outline Dimension (L X W):**
  338.58mm (13.33") X 126.39mm (4.98")

- **Power Requirements:**
  +12V (CPU) @6.96A; +12V (System) @ 0.33A; +5V (System) @0.32A; +3.3V(System) @ 2.49A

System Configuration	
CPU Type	Intel® Xeon® CPU C5539 2.27GHz(ES) Bus Speed:133.3MHz L3:4M
SBC BIOS	Project Version:0ABRB 0.19 x64 Build Date:01/20/2010 10:10:10
Memory	Apacer ECC DDR3-1066 1GB (ELPIDA J1108BDBG-DJ-F)*2
VGA Card	Onboard XGI Volari Z7-Z9-Z9s-Z11 V1.11.03
VGA Driver	XGI Volari Z7-Z9-Z9s-Z11 Version 6.14.10.1110
LAN Card	Onboard Intel® 82574L Gigabit Network Connection
LAN Driver	Intel® 82574L Gigabit Network Connection Version 11.4.7.0
Chip Driver	Intel® Chipset Device Software Version 9.1.2.1002
USB 2.0 Driver	Intel®5 Series/3400 Series Chipset Family USB Enhanced Host Controller Ver:9.1.1.1013
SATA HDD	Seagate ST3160815AS
FDD	Teac 1.44
CDROM	Pioneer DVD-227A
Power Supply	FSP350-60GLC
Back plane	PBPE-06P2

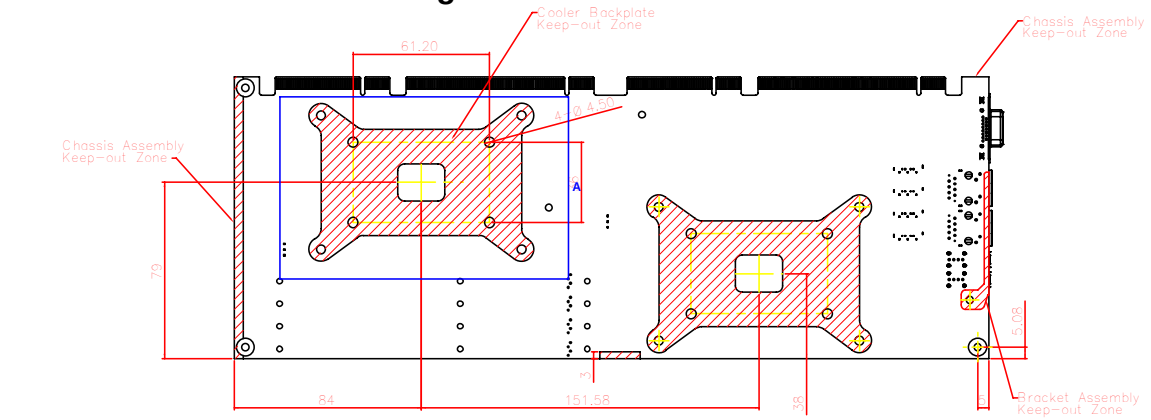
Power Consumption test: Run Burning Test V6.0
RUN time: 30 Minutes.

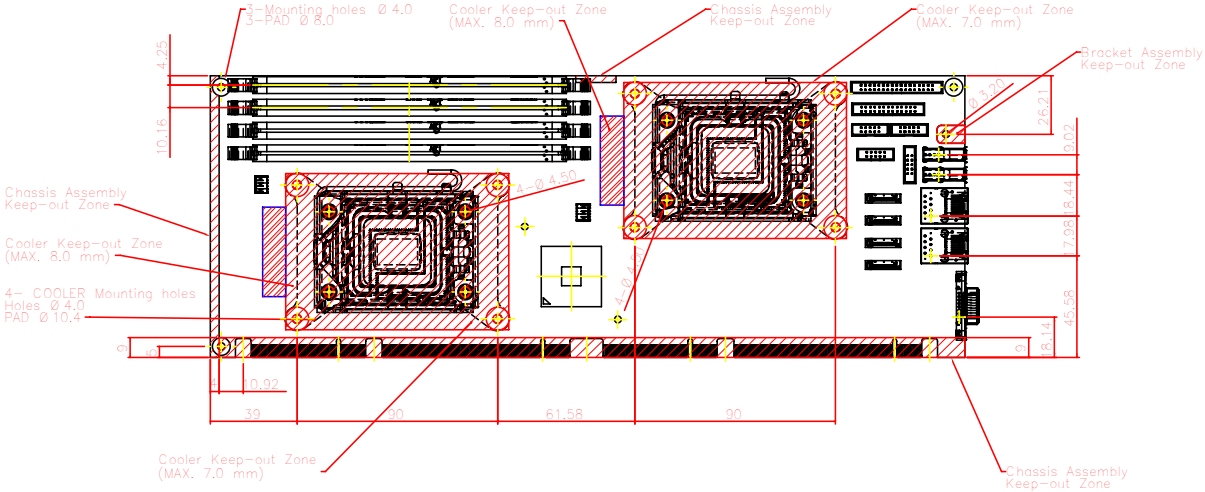
- **Operating Temperature:**
  -5°C ~ 55°C (23°F ~ 131°F)

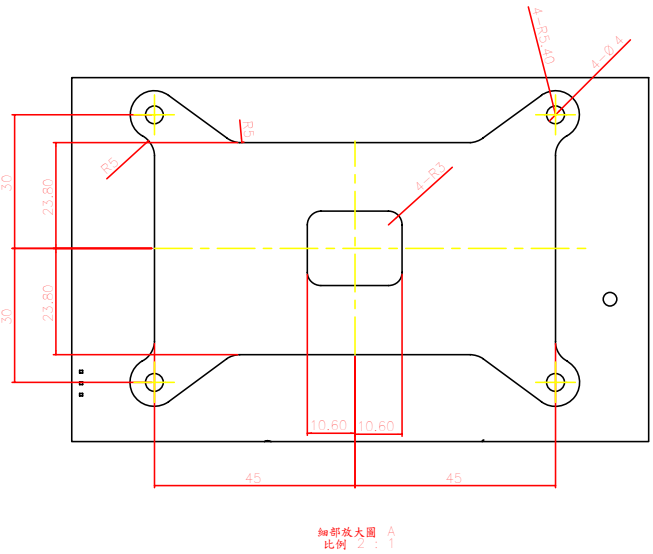
- **Storage Temperature:**
  -20°C ~ 80°C

- **Relative Humidity:**
  0% ~ 90%, non-condensing

1.3.1 Mechanical Drawing







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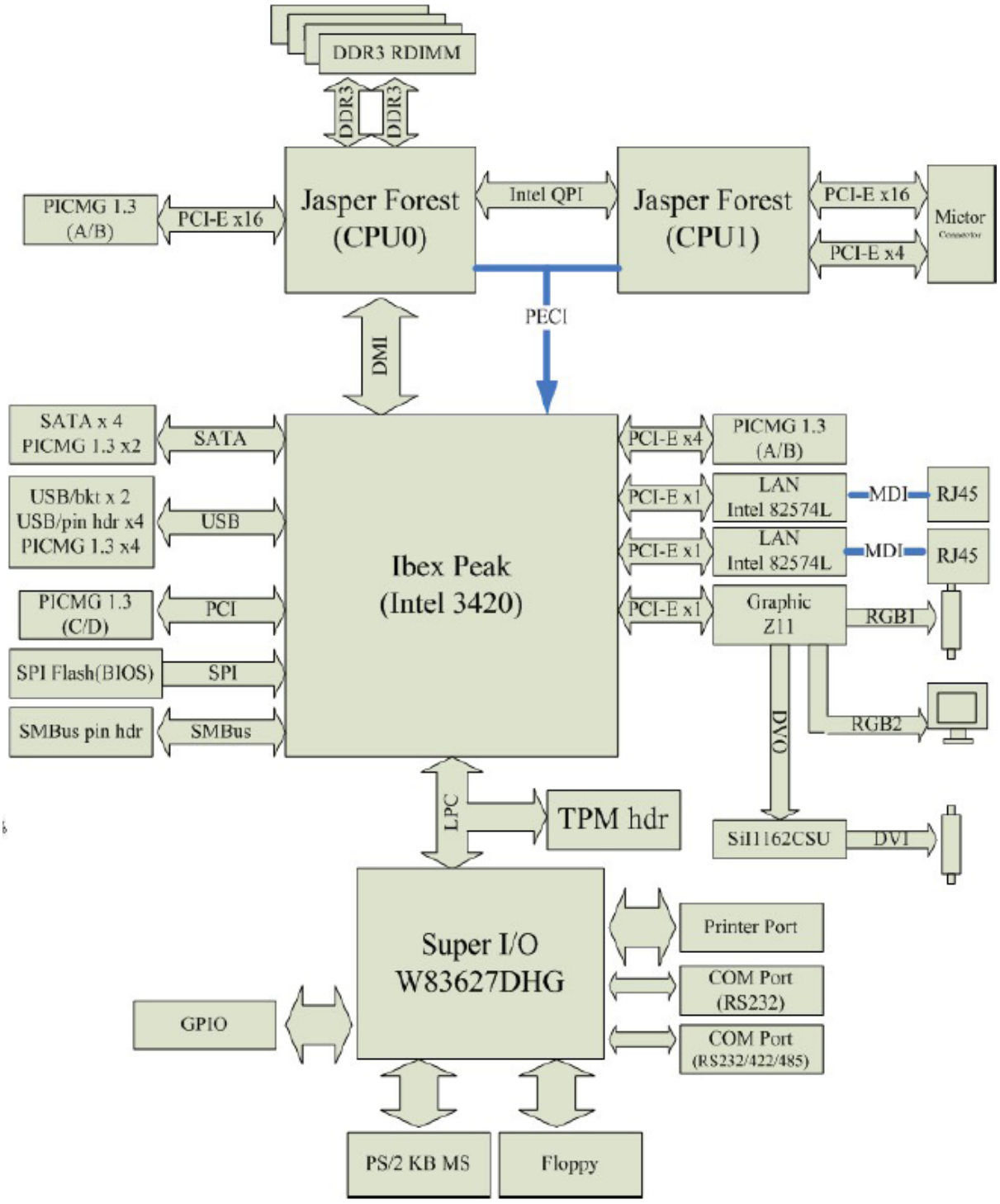
比例 2 : 1

1.4 System Architecture

ROBO-8120VG2R adopts Intel® single or dual Dual-Core™/Quad-Core™ Xeon® C5500/C3500 series processors in LGA1366 package and 3420 server chipset. Intel® Xeon® processors support ECC & registered DDR3 1333/1066/800 system memory up to 32GB on four DIMM sockets, and two configurable PCI Express x8 links. The PCI Express link was configured as four PCI Express x4 and one PCI Express x16 thru BIOS and jumper setting. Two PCI Express x1 links were used to equip Intel® 82574L Gigabit Ethernet Controller which takes advantage of short route to processor and memory to increase it performance. The other three PCI Express x4 and PCI Express x8 links are routed to gold finger for external expansion.

3420 supports one PCI bus which was designed to support external PCI devices and PCI-E x1 bus was for on-board display controller – XGI Z11. XGI Z11 default equipped with 32MB DDR2 memory on-board and scalable to expand to 64MB for higher memory resolution and frequency support. Default configuration of display interface is one VGA connector on bracket, and it can be extended to have 2nd VGA or DVI-D extension. The chipset also features SATA, USB and LPC (Low Pin Count) interface for storage devices and Super I/O connections.

Super I/O – Winbond W83627DHG on LPC provides I/O interfaces such as PS/2 keyboard/mouse, dual serial ports, one parallel port, one FDD channel and functions like WatchDog timer and Hardware Monitoring.



ROBO-8120VG2R System Block Diagram

Chapter 2
Hardware Configuration

This chapter indicates jumpers', headers' and connectors' locations. Users may find useful information related to hardware settings in this chapter. The default settings are indicated with a star sign (★).

2.1 Jumper Setting

In the following sections, Short means covering a jumper cap over jumper pins; Open or N/C (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 2-1 for the Jumper locations.

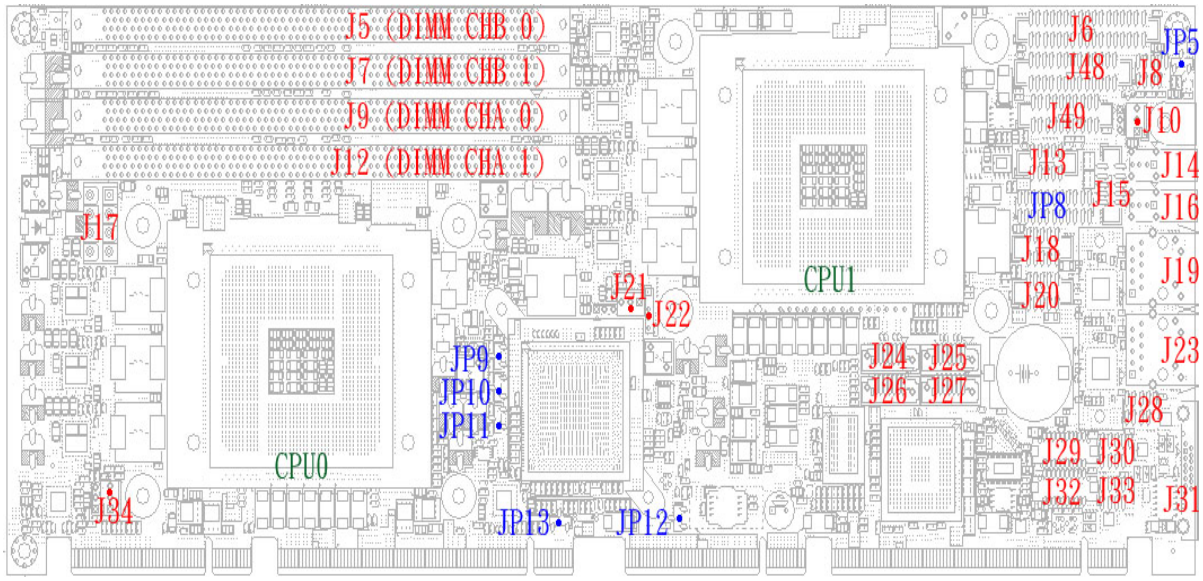


Figure 2-1 ROBO-8120VG2R Top-side Jumper and Connector Locations

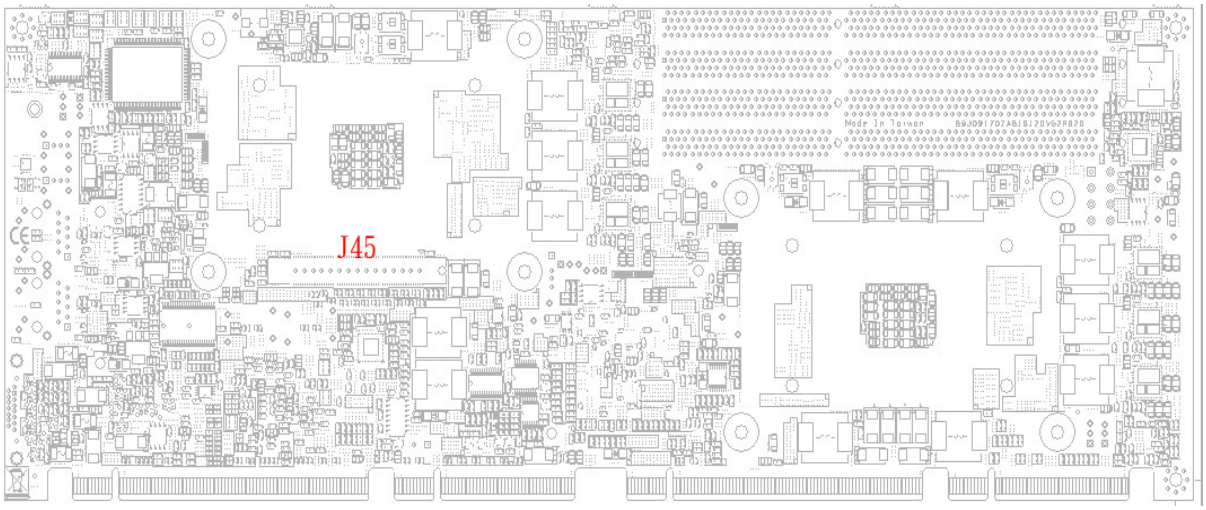


Figure 2-2 ROBO-8120VG2R Bottom-side Jumper and Connector Locations

Jumper List	
JP5	Auto-power button
JP8	RS232/422/485 selection jumper for COM port 2 (J20)
JP9	PECFGSEL2 for PCI-e link width strapping option
JP10	PECFGSEL0 for PCI-e link width strapping option
JP11	PECFGSEL1 for PCI-e link width strapping option
JP12	CMOS normal / clear jumper
JP13	Voltage selection for VIO of PCI slot on backplanes

JP5: Auto power on jumper

JP5	Function
1-2 Short	System boots up automatically with jumper populated after PSU powered.
2-3 Short	System requires power button pushed to boot up without jumper populated. ★

JP8: COM2 (J20) Interface Selection

RS-232

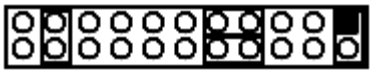
22 20 18 16 14 12 10 8 6 4 2

21 19 17 15 13 11 9 7 5 3 1

RS-422

22 20 18 16 14 12 10 8 6 4 2

21 19 17 15 13 11 9 7 5 3 1



RS-485

22 20 18 16 14 12 10 8 6 4 2

JP8	Function
5-6,9-11,10-12,15-17,16-18 Short	RS-232 ★
3-4,7-9,8-10,13-15,14-16,21-22 Short	RS-422
1-2,7-9,8-10,19-20 Short	RS-485

JP9 / JP10 / JP11 : PECFGSEL[2:0] for PCI-e link width options

JP9, JP10, JP11	Function
1-2 Short	Logic 0.
2-3 Short	Logic 1.

JP9: PECFGSEL2
JP10: PECFGSEL0
JP11: PECFGSEL1

There are 16 PCE-e lanes from CPU0. User may define the configurations with various kinds of PICMG 1.3 backplanes. The configurations are shown as follows.

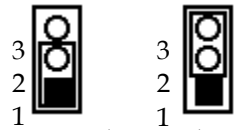
Link Width Strapping Options

PECFGSEL[2:0]	Behavior of PCIe Port
000	Reserved
001	Reserved
010	x8x4x4
011	x4x4x8
100	Wait-On-BIOS
101	x4x4x4x4
110	x8x8
111	x16

JP9 / JP10 / JP11 : PCIe configuration for PICMG 1.3 backplane

JP9	JP11	JP10	x4 x4 x4 x4	**PBPE-06V464** **PBPE-06P4**
JP9	JP11	JP10	x4 x4 x8	
JP9	JP11	JP10	x8 x4 x4 ★	**PBPE-14AD64** **PBPE-19AG64**
JP9	JP11	JP10	x8 x8	**PBPE-06A364** **PBPE-06P2** **PBPE-08P41**
JP9	JP11	JP10	x16	**PBPE-06V3** **PBPE-07P4** **PBPE-05A364** **PBPE-12A9** **PBPE-12AA64** **PBPE-13A8**

JP12: CMOS Normal / Clear Jumper



JP12	Function
1-2 Short	Clear CMOS Disable (Normal) ★
2-3 Short	Clear CMOS Enable (Clear)

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors

Connector List	
J5	DDR3 slot for DIMM0 of channel B
J6	Floppy header
J7	DDR3 slot for DIMM1 of channel B
J8	Front panel header
J9	DDR3 slot for DIMM0 of channel A
J10	System fan header
J12	DDR3 slot for DIMM1 of channel A
J13	PS2 keyboard mouse header
J14	USB connector
J15	GPIO header
J16	USB connector
J17	ATX 12V power supply connector for CPU Vcore
J18	COM port 1 header
J19	LAN port 1
J20	COM port 2 header
J21	CPU1 fan header
J22	SMBus header
J23	LAN port 2
J24	SATA port 0
J25	SATA port 1
J26	SATA port 3
J27	SATA port 2
J28	USB header

J29	DVI header
J30	USB header
J31	VGA2 connector
J32	VGA1 header
J33	USB connector
J34	CPU0 fan header
J45	PCI-e extension port for PCI-e 16+4 lanes from CPU1
J48	LPT
J49	TPM

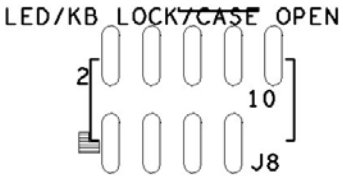
J5, J7, J9, J12: DDR3 DIMM slots

Please insert same type of DDR3 module from DIMM 0 of channel A, then DIMM 0 of channel B if dual channel mode is required.

J6: Floppy header

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Density Select 0
3	Ground	4	N/C
5	Ground	6	N/C
7	Ground	8	INDEX#
9	Ground	10	Motor ENA#
11	Ground	12	N/C
13	Ground	14	Drive Select A#
15	Ground	16	N/C
17	Ground	18	Direction#
19	Ground	20	Step#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 0#
27	Ground	28	Write Protect#
29	N/C	30	Read Data#
31	Ground	32	Head Select#
33	N/C	34	Disk Change#

J8: Front panel header



PIN No.	Signal Description	PIN No.	Signal Description
1	HDD LED (+) w/ 150 ohm 5V pull-up	2	Power LED (+) w/ 330 ohm 5V pull-up
3	HDD LED (-)	4	NC
5	PS2 Keyboard Lock	6	Power LED (-)
7	PS2 Keyboard Lock	8	Case Open
		10	Case Open

J10, J21, J34: System fan header, CPU1 fan header, CPU0 fan header

PIN No.	Signal Description
1	Ground
2	Fan Power (12V maximum)
3	Fan PWM Input

J13: PS2 keyboard mouse header

PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Data
3	NC	4	NC
5	Ground	6	Ground
7	Mouse Power	8	Keyboard Power
9	Mouse Clock	10	Keyboard Clock

PS. PS2 KB/MS function will be ready from R1 version only.

J15: GPIO header

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO30 (From SUPER I/O)	2	GPIO34 (From SUPER I/O)
3	GPIO31 (From SUPER I/O)	4	GPIO35 (From SUPER I/O)
5	GPIO22 (From SUPER I/O)	6	GPIO36 (From SUPER I/O)
7	GPIO23 (From SUPER I/O)	8	GPIO37 (From SUPER I/O)
9	Ground	10	5V

J17: ATX 12V power supply connector for CPU Vcore

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Ground
3	Ground	4	Ground
5	12V	6	12V
7	12V	8	12V

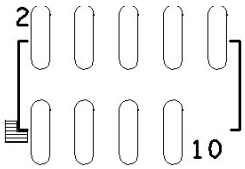
J18, J20: COM port 1, COM port 2

Pin No.	Signal Description
1	Data Carrier Detect
2	Data Set Ready
3	Receive Data
4	Request To Send
5	Transmit Data
6	Clear To Send
7	Data Terminal Ready
8	Ring Indicator
9	Ground
10	NC

J22: SMBus header

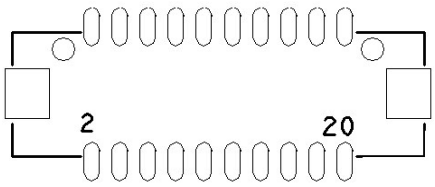
Pin No.	Signal Description
1	SMBus clock
2	NC
3	Ground
4	SMBus data
5	3.3V

J28, J30: USB header



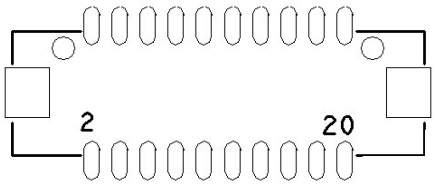
PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	+5V
3	DATA-	4	DATA-
5	DATA+	6	DATA+
7	Ground	8	Ground
		10	Ground

J29: DVI header



PIN No.	Signal Description	PIN No.	Signal Description
1	TX0N	2	TX0P
3	Ground	4	Ground
5	TX1N	6	TX1P
7	Ground	8	Ground
9	TX2N	10	TX2P
11	Ground	12	Ground
13	TXCN	14	TXCP
15	Ground	16	Ground
17	DVI I2C Clock	18	DVI I2C Data
19	Hot Plug Detection	20	NC

J32: VGA1 header



PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	5V
3	Red	4	5V
5	Ground	6	NC
7	Green	8	Ground
9	Ground	10	VGA I2C data
11	Blue	12	VGA I2C clock
13	Ground	14	Ground
15	Hsync	16	NC
17	Ground	18	Ground
19	Vsync	20	NC

J48 LPT

PIN No.	Signal Description	PIN No.	Signal Description
1	STB#	14	Ground
2	AFD#	15	Data 6
3	Data 0	16	Ground
4	ERR#	17	Data 7
5	Data 1	18	Ground
6	INT#	19	ACK#
7	Data 2	20	Ground
8	SLIN#	21	BUSY
9	Data 3	22	Ground
10	Ground	23	PE
11	Data 4	24	Ground
12	Ground	25	SLCT
13	Data 5	26	Ground

J49 TPM

PIN No.	Signal Description	PIN No.	Signal Description
1	CLK_TPM_33M	2	GND
3	LPC_FRAME_N	4	NC
5	PLTRST_TPM_N	6	VCC5
7	LPC_LAD3	8	LPC_LAD2
9	VCC3	10	LPC_LAD1
11	LPC_LAD0	12	GND
13	SMB_PCH_3V3SB_CLK	14	SMB_PCH_3V3SB_DAT
15	VCC3P3_AUX	16	IRQ_SERIAL
17	GND	18	NC
19	PCH_SUS_STAT_N	20	NC

Chapter 3
System Installation

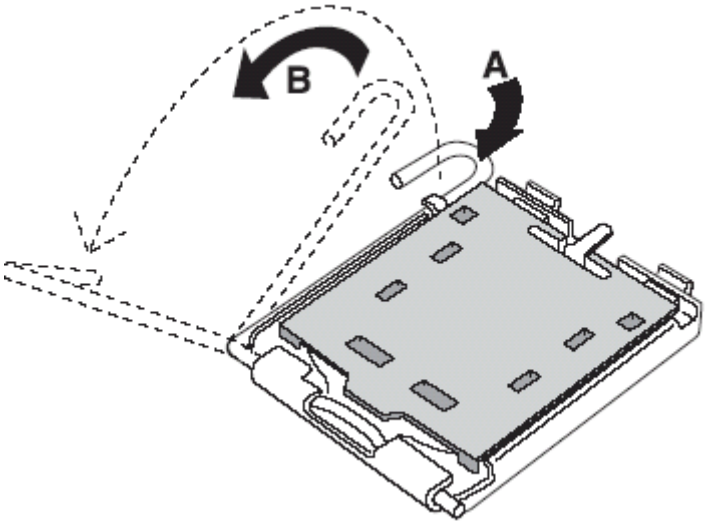
This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel® LGA 1366 Processor

Installing LGA 1366 CPU

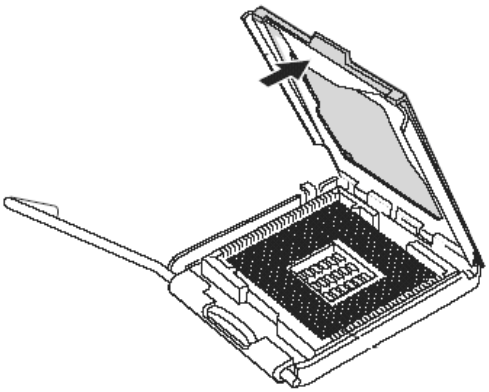
Brand	Processor Number	Architecture			Clock Speed (GHz)	Front Side Bus (MHz)	QPI (GT/s)	Last Level Cache	Ideal for ATCA / NEBS (Tcase)	TDP	Intel Technologies					
		Processor Generation	Process	Socket							Cores	Intel® VT	HT	Enhanced Intel SpeedStep® Technology	Intel® 64	Execute Disable Bit
	EC5549	Jasper Forest	45 nm	LGA1366	2.53		5.86	8MB		85W	4	√	√	√	√	√
	EC5509	Jasper Forest	45 nm	LGA1366	2		4.8	8MB		85W	4	√		√	√	√
	LC5528	Jasper Forest	45 nm	LGA1366	2.13		4.8	8MB	√	60W	4	√	√	√	√	√
	EC5539	Jasper Forest	45 nm	LGA1366	2.27		5.86	4MB		65W	2	√		√	√	√
	LC5518	Jasper Forest	45 nm	LGA1366	1.73		4.8	8MB	√	48W	4	√	√	√	√	√
	EC3539	Jasper Forest	45 nm	LGA1366	2.13		4.8	8MB		65W	4	√		√	√	√
	TBD	Jasper Forest	45 nm	LGA1366	1.33		4.8	2MB		30W	1	√	√	√	√	√
	LC3528	Jasper Forest	45 nm	LGA1366	1.73		4.8	4MB	√	32W	2	√	√	√	√	√
	LC3518	Jasper Forest	45 nm	LGA1366	1.73		4.8	2MB	√	23W	1	√		√	√	√

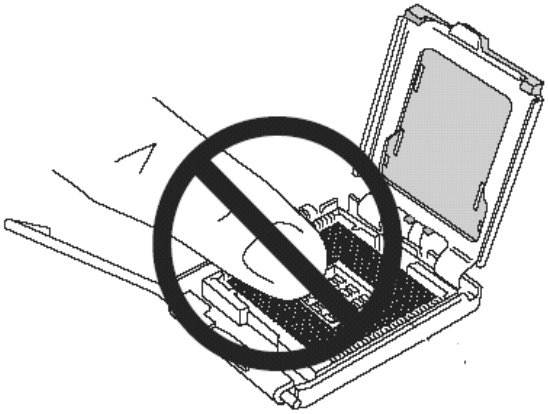
Lift the handling lever of CPU socket outwards and upwards to the other end.



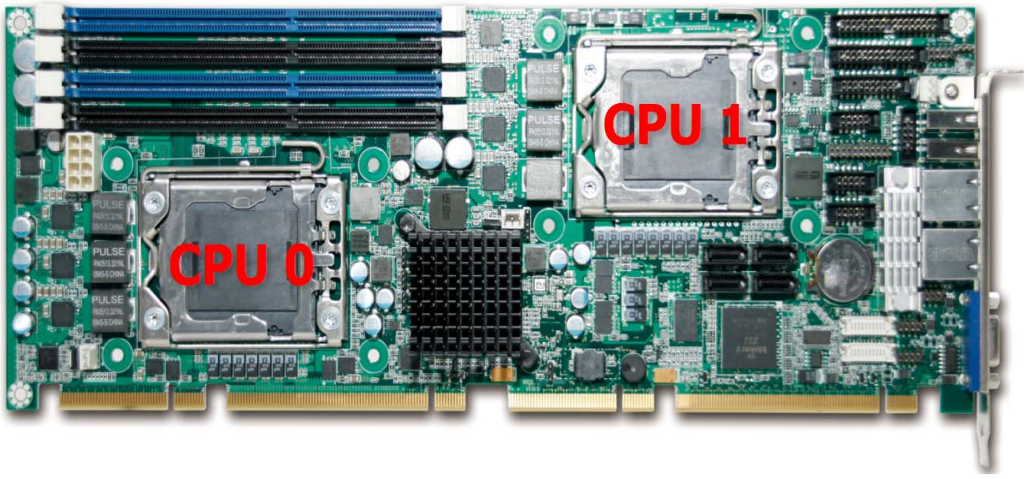
Align the processor pins with pinholes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place . If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.

Triangle mark is meaning first pin position; kindly assemble and take aim at notch of top and bottom between CPU and socket.





If you only need one processor in your platform, please install it on CPU 0.



Note:
Don't touch directly by your hand or impacts internal align balls of CPU socket to avoid motherboard destruction, it is a precise actuator.

3) Push down the lever to lock processor chip into the socket once CPU fits.

4) Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the LGA 1366 socket.

Removing CPU

1) Unlock the cooling fan first.
2) Lift the lever of CPU socket outwards and upwards to the other end.
3) Carefully lifts up the existing CPU to remove it from the socket.
4) Follow the steps of installing a CPU to change to another one or place handling bar to close the opened socket.

Configuring System Bus

ROBO-8120VG2R will automatically detect the CPU FSB 800/1066/1333 MHz used. CPU speed of Intel Core 2 Duo and Intel Core 2 Quad Processor can be detected automatically.

Inserting Memory Module

We suggest you to insert the memory from DIMM0 to DIMM3 sequentially when you have one more memory for using. When you use only one memory in system, we suggest to insert in DIMM 0. If you want to use the channel A- slot 2, you must use channel A- slot 1 first. Otherwise, the system can't boot. The Channel B has the same rule.

DIMM3	ECC DDR3 DIMM channel B - slot 2
DIMM2	ECC DDR3 DIMM channel B - slot 1
DIMM1	ECC DDR3 DIMM channel A - slot 2
DIMM0	ECC DDR3 DIMM channel A - slot 1

3.2 Main Memory

ROBO-8120VG2R provide 4 x 240-pin DIMM sockets which supports 800/1066/1333 ECC DDR3 SDRAM as main memory, The maximum memory size can be up to 32GB capacity.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be either one double-sided DIMM in either one DIMM socket or two single-sided DIMM in both sockets.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

Dual Channel DDR3 DIMM

Dual Channel DDR3 memory technology doubles the bandwidth of memory bus. Adequate or higher bandwidth of memory than processor would increase system performance. To enable Dual Channel DDR3 memory technology, you have to install dual identical memory modules in both memory sockets. Following tables show bandwidth information of different processor and memory configurations.

CPU FSB	Bandwidth
1333MHz	10.6GB/s
1066MHz	8.5GB/s
800MHz	6.4GB/s

Memory Frequency	Dual Channel DDR Bandwidth	Single Channel DDR Bandwidth
1333MHZ	21.2GB/s	10.6GB/s
1066MHz	17GB/s	8.5GB/s
800MHz	12.8GB/s	6.4GB/s

Note:
To maintain system stability, don't change any of DRAM parameters in BIOS setup to upgrade system performance without acquiring technical information.

3.3 Installing the Single Board Computer

To install your ROBO-8120VG2R into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place ROBO-8120VG2R into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING
Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.3.1 to 3.3.7 to install INF/VGA/LAN/Audio/Raid & TPM drivers.

3.3.1 Chipset Component Driver

The chipset on ROBO-8120VG2R is a new chipset that a few old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP/Vista/Win7, please install its INF before any of other Drivers are installed. You can select the Intel Chipset driver from the ROBO-8120VG2R CD-title.

3.3.2 Intel Integrated Graphics GMCH Chip

ROBO-8120VG2R comes with the XGI Z11 graphics supporting. Shared 32 accompany it to 256MB system Memory with Total Graphics Memory. This combination makes ROBO-8120VG2R an excellent piece of multimedia hardware.

With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI-Express by 16 VGA card can take over the system display.

Drivers Support

Please select Graphic driver from the ROBO-8120VG2R Driver CD-title. Driver supports Windows XP/Vista/Win7.

3.3.3 On-board Fast Ethernet Controllers

Drivers Support

Please select Intel Ethernet driver from the ROBO-8120VG2R Driver CD-title to install those two integrated Intel® 82574L Gigabit Ethernet controller drivers. Those two drivers support Windows XP/Vista/Win7.

LED Indicator (for LAN status)

This provides two LED indicators to report Dual Intel 82574L Gigabit Ethernet interface status. Please refer to the table below as a quick reference guide.

<table>
<tr><th rowspan="2">82574L</th><th rowspan="2">Color</th><th rowspan="2">Name of LED</th><th colspan="3">Operation of Ethernet Port</th></tr>
<tr><th colspan="2">Linked</th><th>Active</th></tr>
<tr><td>Status LED</td><td>Orange</td><td>LAN Linked & Active LED</td><td colspan="2">On</td><td>Blinking</td></tr>
<tr><td rowspan="2">Speed LED</td><td>Orange</td><td rowspan="2">LAN speed LED</td><td>Giga Mbps</td><td>100 Mbps</td><td>10 Mbps</td></tr>
<tr><td>Green</td><td>Orange</td><td>Green</td><td>Off</td></tr>
</table>

3.3.4 On-board High Definition Audio Controller

Drivers Support

Please select the Realtek High Definition Codec Audio driver form ROBO-8120VG2R Driver CD-title. The driver supports Windows XP/Vista/Win7.

3.3.5 Intel Matrix Storage Manager Device

Drivers Support

Please find utility tool for Intel 3420 of ROBO-8120VG2R CD-title. The drivers support Windows XP/Vista/Win7.

Installing Serial ATA hard disks

The ROBO-8120VG2R supports Four Serial ATA hard disk drives. For optimal performance, install identical drives of the same model and capacity when creating a disk array.

To install the SATA hard disks for a RAID configuration:
1. Install the SATA hard disks into the drive bays.
2. Connect the SATA signal cables.
3. Connect a SATA power cable to the power connector on each drive.

Intel RAID configurations

This ROBO-8120VG2R supports RAID 0, RAID 1, RAID 5, RAID (1+0) and Intel® Matrix Storage configurations for Serial ATA hard disks drives through the Intel 3420 chipset.

RAID configurations

RAID 0 (Data striping) optimizes two identical hard disk drives to read and write data in parallel, interleaved stacks. Two hard disks perform the same work as a single drive but at a sustained data transfer rate, double that of a single disk alone, thus improving data access and storage. Use of two new identical hard disk drives is required for this setup.

RAID 1 (Data mirroring) copies and maintains an identical image of data from one drive to a second drive. If one drive fails, the disk array management software directs all applications to the surviving drive as it contains a complete copy of the data in the other drive. This RAID configuration provides data protection and increases fault tolerance to the entire system. Use two new drives or use an existing drive and a new drive for this setup. The new drive must be of the same size or larger than the existing drive.

RAID 5 stripes both data and parity information across three or more hard disk drives. Among the advantages of RAID 5 configuration include better HDD performance, fault tolerance, and higher storage capacity. The RAID 5 configuration is best suited for transaction processing, relational database applications, enterprise resource planning, and other business systems. Use a minimum of three identical hard disk drives for this setup.

RAID 10 is data striping and data mirroring combined without parity (redundancy data) having to be calculated and written. With the RAID 10 configuration you get all the benefits of both RAID 0 and RAID 1 configurations. Use four new hard disk drives or use an existing drive and three new drives for this setup.

Intel Matrix Storage Manager. The Intel® Matrix Storage technology supported by the 3420 chip allows you to create a RAID 0 and a RAID 1 set using only two identical hard disk drives. The Intel® Matrix Storage technology creates two partitions on each hard disk drive to create a virtual RAID 0 and RAID 1 sets. This technology also allows you to change the hard disk drive partition size without losing any data.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP12: CMOS Clear

JP12	Function
1-2 Short	Clear CMOS Disable (Normal) ★
2-3 Short	Clear CMOS Enable (Clear)

3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

ROBO-8120VG2R allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to Winbond W83627DHG data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,
1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

Below are some example codes, which demonstrate the use of WDT.

```
//Enter W83627DHG configuration registers mode

outp(0x2E, 0x87);
outp(0x2E, 0x87);

//Assign Pin77 to be WDTO#
outp(0x2E, 0x2D);
outp(0x2E + 1, inp(0x002E + 1) & 0xFE);

//Select logic device 8
outp(0x2E, 0x07);
outp(0x2E + 1, 0x08);
```

```
// Select Count Mode (Minute or Second)
outp(0x002E, 0xF5);
outp(0x002F, (inp(0x002F) & 0xF7) | ( Count-mode Register & 0x08));

// Specify Time-out Value
outp(0x002E, 0xF6);
outp(0x002F, Time-out Value Register );

// Disable WDT reset by keyboard/mouse interrupts
outp(0x002E, 0xF7);
outp(0x002F, 0x00);

// Exit Extended Function Mode
outp(0x002E, 0xAA);
```

Definitions of Variables:
Value of Count-mode Register :
1) 0x00 -- Count down in seconds (Bit3=0)
2) 0x08 -- Count down in minutes (Bit3=1)
Value of Time-out Value Register :
1) 0x00 -- Time-out Disable
2) 0x01~0xFF -- Value for counting down

3.6 GPIO

The ROBO-8210VG2R provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

3.6.1 Pin assignment

- **J15: GPIO header**

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO30 (From SUPER I/O)	2	GPIO34 (From SUPER I/O)
3	GPIO31 (From SUPER I/O)	4	GPIO35 (From SUPER I/O)
5	GPIO22 (From SUPER I/O)	6	GPIO36 (From SUPER I/O)
7	GPIO23 (From SUPER I/O)	8	GPIO37 (From SUPER I/O)
9	Ground	10	5V

All General Purpose I/O ports can only apply to standard TTL ± 5% signal level (0V/5V), and each source sink capacity up to 12mA.

3.6.2 ROBO-8120VG2R GPIO Programming Guide

There are 8 GPIO pins on ROBO-8120VG2R. These GPIO pins are from SUPER I/O (W83627DHG) GPIO pins, and can be programmed as Input or Output direction.

J15 pin header is for 8 GPIO pins and its pin assignment as following :

J15_Pin1=GPIO0:from SUPER I/O_GPIO30 with Ext. 4.7K PH
J15_Pin2=GPIO1:from SUPER I/O_GPIO34 with Ext. 4.7K PH
J15_Pin3=GPIO2:from SUPER I/O_GPIO31 with Ext. 4.7K PH
J15_Pin4=GPIO3:from SUPER I/O_GPIO35 with Ext. 4.7K PH
J15_Pin5=GPIO4:from SUPER I/O_GPIO22 with Ext. 4.7K PH
J15_Pin6=GPIO5:from SUPER I/O_GPIO36 with Ext. 4.7K PH
J15_Pin7=GPIO6:from SUPER I/O_GPIO23 with Ext. 4.7K PH
J15_Pin8=GPIO7:from SUPER I/O_GPIO37 with Ext. 4.7K PH

<<<<< Be careful Pin9=GND , Pin10=VCC >>>>>

There are several Configuration Registers (CR) of W83627DHG needed to be programmed to control the GPIO direction, and status(GPI)/value(GPO). CR00h ~ CR2F are common (global) registers to all Logical Devices (LD) in W83627DHG. CR07h contains the Logical Device Number that can be changed to access the LD as needed. LD7 contains the GPIO10~17 registers.

Programming Guide:

Step1: CR2C_Bit [7..5]. P [1,1,1]; to select multiplexed pins as GPIO32~34 pins
Step2: LD7_CR07h.P [09h]; Point to LD9
Step3: LD7_CR30h_Bit1.P1; Enable GPIO3
Step4: Select GPIO direction, Get Status or output value.

LD9_CRF0h; GPIO37~30 direction, 1 = input, 0 = output pin
LD9_CRF2h.P [00h]; Let CRF1 (GPIO data port) non-invert to prevent from confusion

LD9_CRF1h; GPIO37~30 data port, for input pin, get status from the related bit, for output pin, write value to the related bit.

For example,
LD9_CRF0h_Bit4.P0; Let GPIO34 as output pin
LD9_CRF2h_Bit4.P0; Let CRF1_Bit4 non-inverted
LD9_CRF1h_Bit4.P0; Output "0" to GPIO34 pin (J13_Pin1)

LD9_CRF0h_Bit0.P1; Let GPIO30 as input pin
LD9_CRF2h_Bit0.P0; Let CRF1_Bit0 non-inverted
Read LD9_CRF1h_Bit0; Read the status from GPIO30 pin (J13_Pin2)

How to access W83627DHG CR?

In ROBO-8120VG2R, the EFER = 002Eh, and EFDR = 002Fh.
EFER and EFDR are 2 IO ports needed to access W83627HG CR.
EFER is the Index Port, EFDR is the Data Port.
CR index number needs to be written into EFER first,
Then the data will be read/written from/to EFDR.

To R/W W83627HG CR, it is needed to Enter/Enable Configuration Mode first.
When completing the programming, it is suggested to Exit/Disable Configuration Mode.

Enter Configuration Mode: Write 87h to IO port EFER twice.
Exit Configuration Mode: Write AAh to IO port EFER.

3.6.3 Example

```
#include <stdio.h>
#include <stdlib.h>
#include <conio.h>
void WDT_Enable(int time,int mode);
void WDT_Disable();
void GPIO_Set_Mode1(int bit,int mode);
void GPIO_Set_Mode2(int bit,int mode);
void GPIO_Write1(int bit,int data);
void GPIO_Write2(int bit,int data);
int GPIO_Read1(int bit);
int GPIO_Read2(int bit);

void main(){
        outp (0x2e,0x87);//Input SIO entry key
        outp (0x2e,0x87);

        //WDT sample code
        WDT_Enable(20,0);
        //WDT_Disable();

        //GPIO sampe code
        GPIO_Set_Mode2(0,0);//set GPIO 30 for output
        GPIO_Set_Mode2(1,1);//set GPIO 31 for input
        GPIO_Set_Mode1(2,1);//Set GPIO 22 for input
        GPIO_Write2(0,1);//Set GPIO 30 for high

        outp (0x2e,0xAA);//Input SIO Exit key
```

```
	return;
}
// time<255   , mode 0 =sec, 1 =min
void WDT_Enable(int time,int mode){

	outp (0x2e,0x2d);
	outp (0x2f,inp(0x2f)&0xfe);//Enable WDT function

	outp (0x2e,0x07);
	outp (0x2f,0x08); //entry device 8

	outp (0x2e,0xF5);
	outp (0x2f,inp(0x2f)|(mode*0x08)); //bit3 0:second,1 Minute

	outp (0x2e,0xf6);
	outp (0x2f,time);// Set time (sec/min)

	outp (0x2e,0xf7);
	outp (0x2f,inp(0x2f)|0xc0);//enable reset time by mouse/keyboard
interrupt

}
void WDT_Disable(){

	outp (0x2e,0x2d);
	outp (0x2f,inp(0x2f)|0x01);//Disable WDT function
}
//bit 2~3=GPIO 22~23, mode 0=output 1=input
void GPIO_Set_Mode1(int bit,int mode){
	int tmp=1<<bit;
	if(bit != 0x02){
	return;
	}
	else if(bit != 0x03){

	return;
	}
	outp (0x2e,0x07);
	outp (0x2f,0x09);// entry device 9

	outp (0x2e,0xE3);
	outp (0x2f,(inp(0x2f)&~tmp)|(tmp*mode));//0 for output,1 for intput
}
//bit 0~1=GPIO 30,31, bit 3~7=GPIO 3~37, mode 0=output 1=input
void GPIO_Set_Mode2(int bit,int mode){
	int tmp=1<<bit;
```

```
	if(bit != 0x02){
	return;
	}
	outp (0x2e,0x07);
	outp (0x2f,0x09);// entry device 9

	outp (0x2e,0xf0);
	outp (0x2f,(inp(0x2f)&~tmp)|(tmp*mode));//0 for output,1 for intput
}

//bit 2~3=GPIO 22~23,data 0 for low, 1 for high
void GPIO_Write1(int bit,int data){
	int tmp=1<<bit;
	if(bit != 0x02){
	return;
	}
	else if(bit != 0x03){
	return;
	}
	outp (0x2e,0x07);
	outp (0x2f,0x09);// entry device 9

	outp (0x2e,0xe4);
	outp (0x2f,(inp(0x2f)&~tmp)|(tmp*data));//0 for low,1 for high

}

//bit 0~1=GPIO 30,31, bit 3~7=GPIO 3~37,data 0 for low, 1 for high
void GPIO_Write2(int bit,int data){
	int tmp=1<<bit;
	if(bit != 0x02){
	return;
	}
	outp (0x2e,0x07);
	outp (0x2f,0x09);// entry device 9

	outp (0x2e,0xf1);
	outp (0x2f,(inp(0x2f)&~tmp)|(tmp*data));//0 for low,1 for high

}
//bit 2~3=GPIO 22~23,high return 1, low return 0, if not GPIO22~23, return 0
int GPIO_Read1(int bit){
	int tmp=1<<bit;
	int data;
	if(bit != 0x02){
	return 0;
```

```
	}
	else if(bit != 0x03){
	return 0;
	}
	outp (0x2e,0x07);
	outp (0x2f,0x09);// entry device 9

	outp (0x2e,0xe4);
	data=inp(0x2f)&~tmp;//read bit

	if (data==0)
		return 0;
	else
		return 1;


}

//bit 0~1=GPIO 30,31, bit 3~7=GPIO 3~37,high return 1, low return 0, if not GPIO
30,31, 33~37, return 0
int GPIO_Read2(int bit){
	int tmp=1<<bit;
	int data;
	if(bit != 0x02){
	return 0;
	}
	outp (0x2e,0x07);

	outp (0x2f,0x09);// entry device 9

	outp (0x2e,0xf1);
	data=inp(0x2f)&~tmp;//read bit

	if (data==0)
		return 0;
	else

		return 1;


}
```

Chapter 4
BIOS Setup Information

ROBO-8210VG2R uses AMI BIOS strutcure stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, ROBO-8210VG2R communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

4.1 Entering Setup -- Launch System Setup

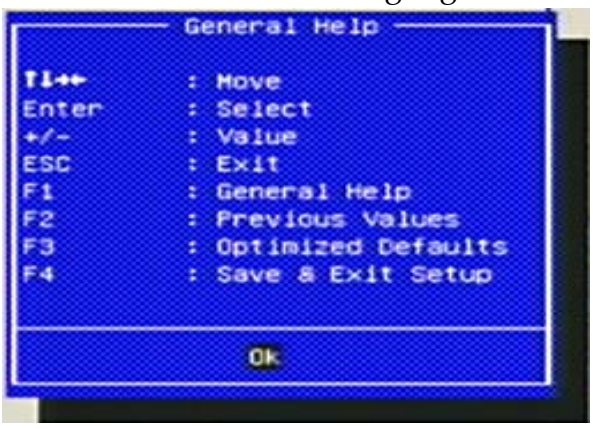
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

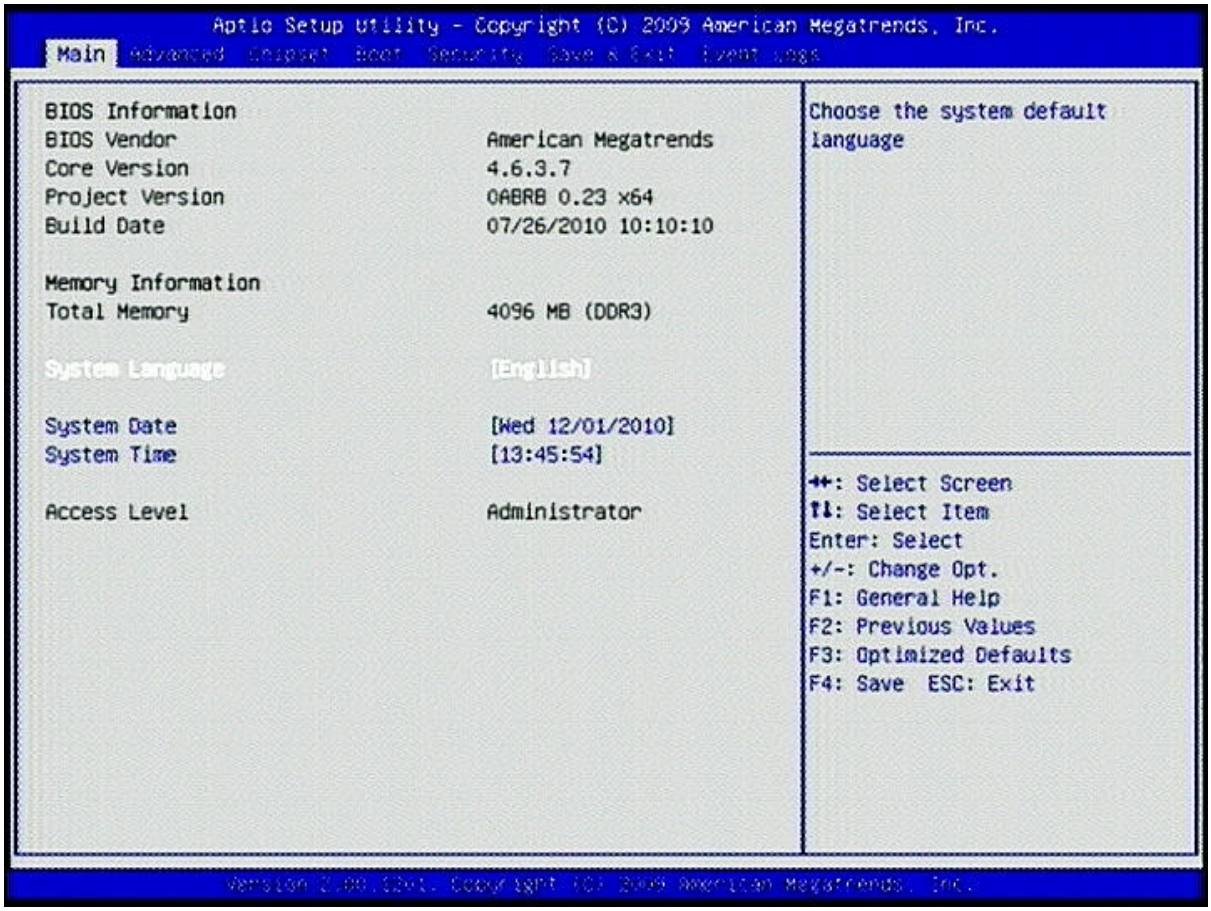
Press <F1> to Run SETUP or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main

Use this menu for basic system configurations, such as time, date etc.



BIOS Information, Memory Information

These items show the firmware and memory specifications of your system. Read only.

System Date

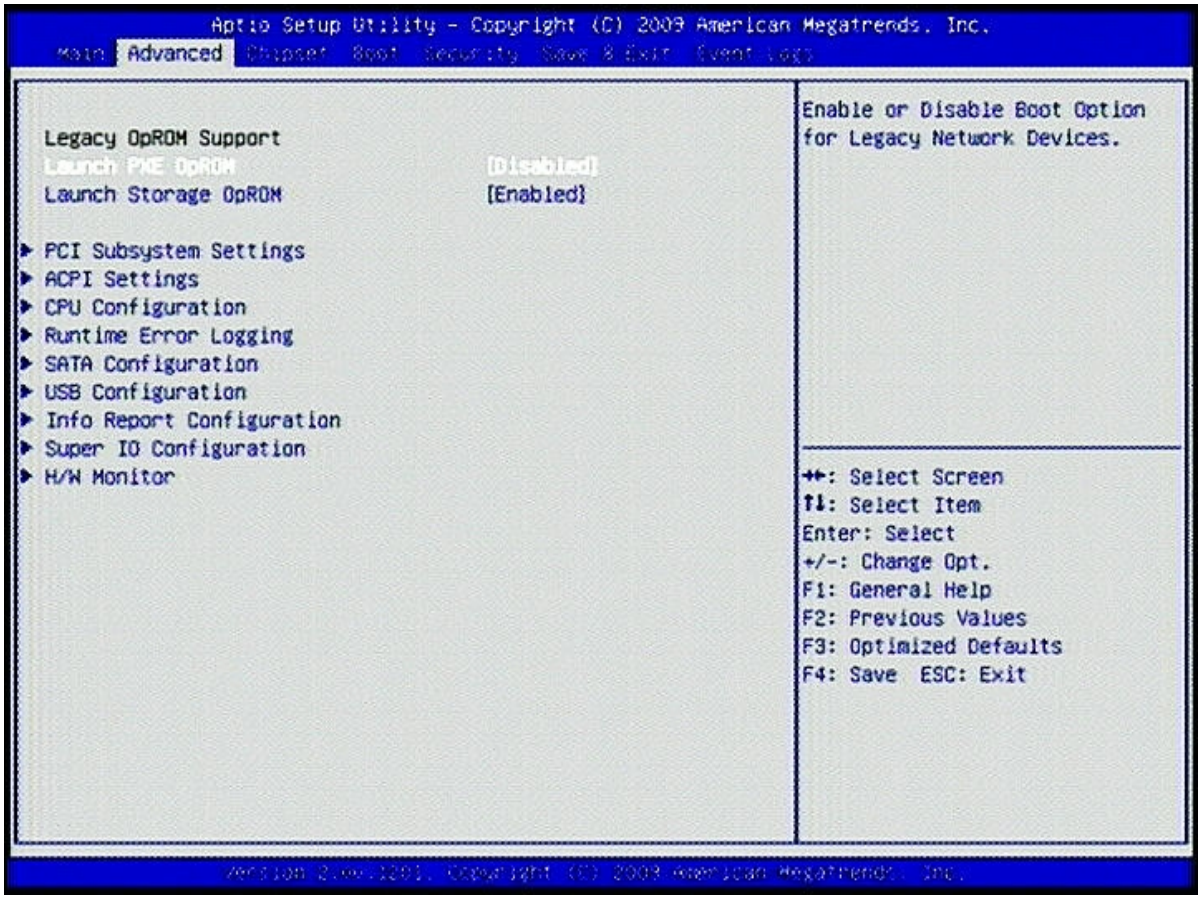
The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

System Time

The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

4.3 Advanced

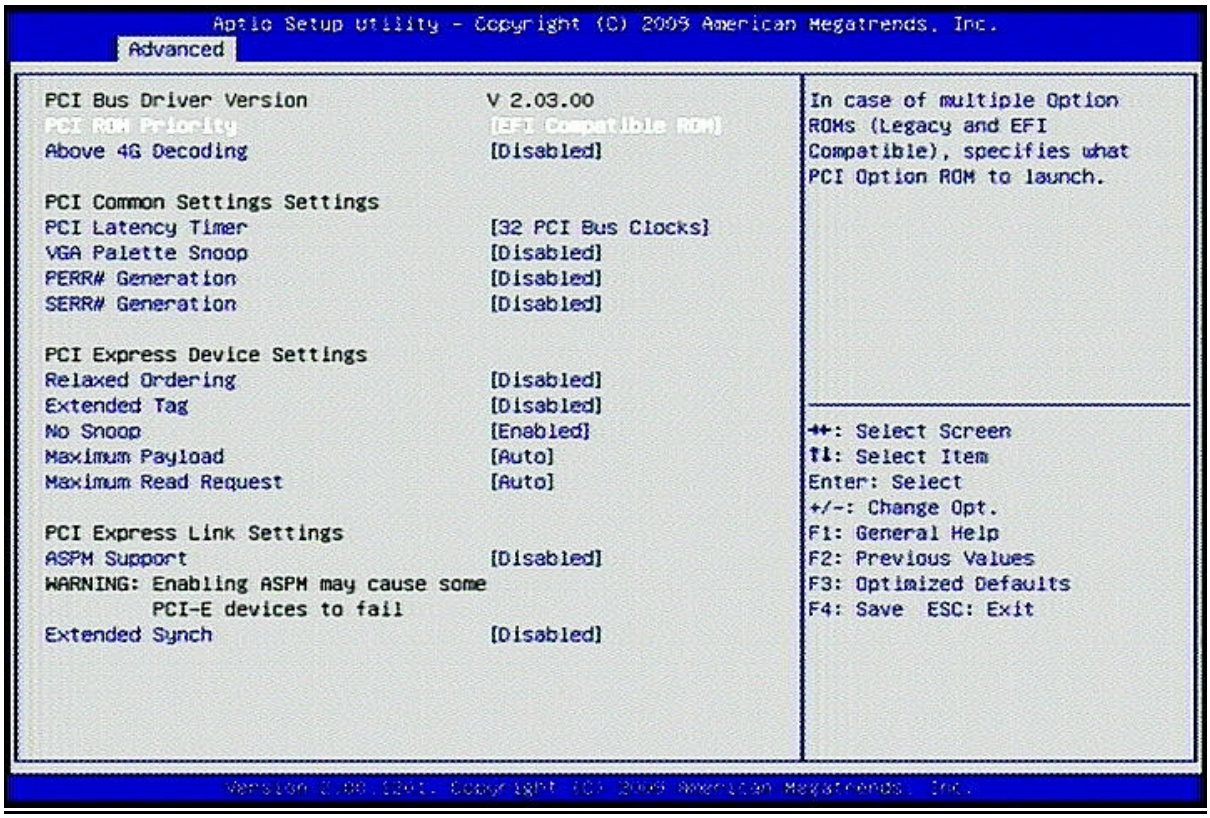
Use this menu to set up the items of special enhanced features.



Launch PXE OpROM
Enable of Disable Boot Option for Lagacy Network Devices.
Choices: Disabled, Enabled

Launch Storage OpROM
Enable of Disable Boot Option for Lagacy Mass Storage devices.
Choices: Disabled, Enabled

PCI Susystems Settings


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
PCI Bus Driver Version V 2.03.00
PCI ROM Priority [EFI Compatible ROM]
Above 4G Decoding [Disabled]
PCI Common Settings Settings
PCI Latency Timer [32 PCI Bus Clocks]
VGA Palette Snoop [Disabled]
PERR# Generation [Disabled]
SERR# Generation [Disabled]
PCI Express Device Settings
Relaxed Ordering [Disabled]
Extended Tag [Disabled]
No Snoop [Enabled]
Maximum Payload [Auto]
Maximum Read Request [Auto]
PCI Express Link Settings
ASPM Support [Disabled]
WARNING: Enabling ASPM may cause some
PCI-E devices to fail
Extended Synch [Disabled]
In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

PCI ROM Priority
Choices: Legacy ROM, EFI Compatible ROM

Above 4G Decoding
Choices: Disabled, Enabled

PCI Latency Timer
Choices: 32 PCI, 64 PCI, 96 PCI, 128 PCI, 160 PCI, 192 PCI, 224 PCI, 248 PCI Bus Clocks

VGA Palette Snoop
Choices: Disabled, Enabled

PERR# Generation
Choices: Disabled, Enabled

SERR# Generation
Choices: Disabled, Enabled

Relaxed Ordering
Choices: Disabled, Enabled

Extended Tag
Choices: Disabled, Enabled

No Snoop
Choices: Disabled, Enabled

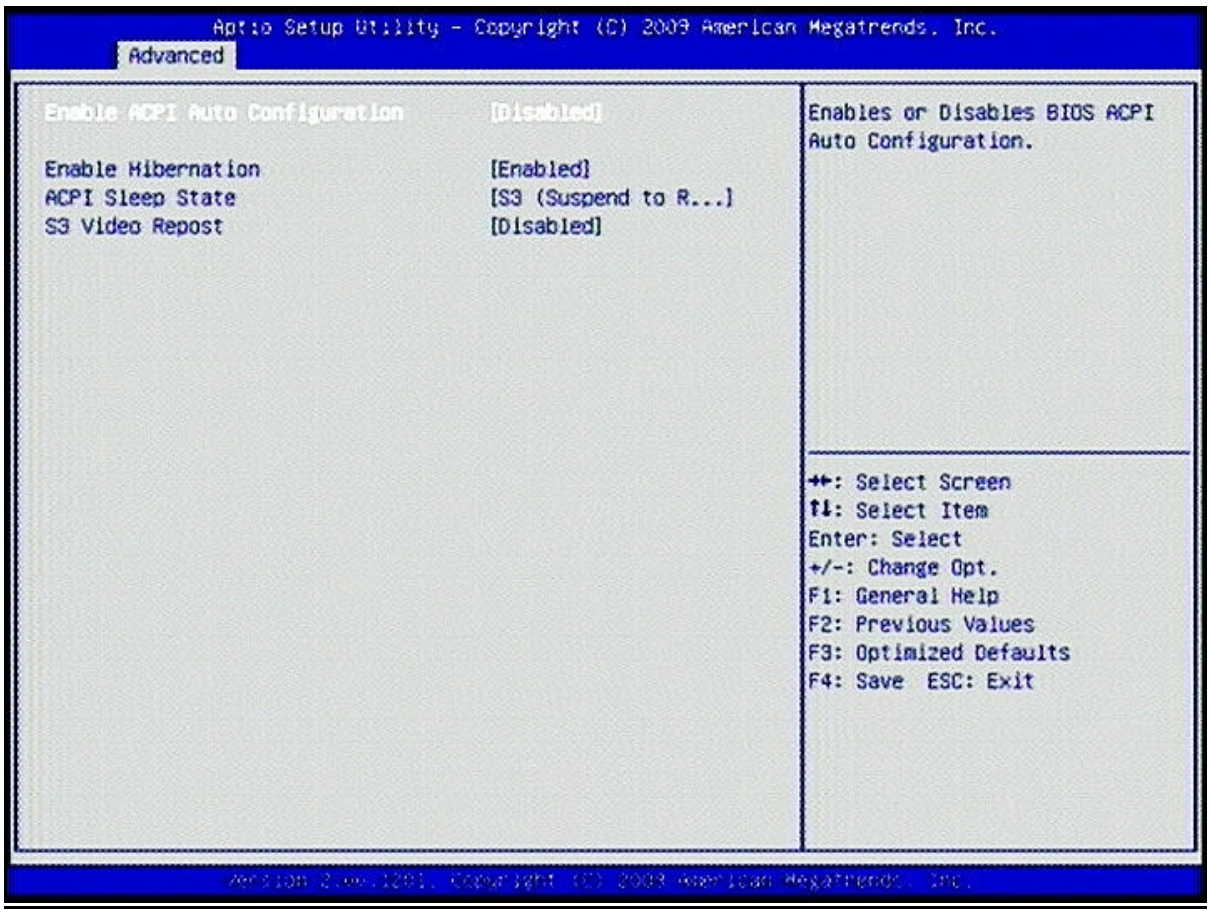
Maximum Payload
Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes

Maximum Read Request
Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes

ASPM Support
Choices: Disabled. Auto, Force L0

Extended Synch
Choices: Disabled, Enabled

ACPI Settings


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Enable ACPI Auto Configuration [Disabled]
Enable Hibernation [Enabled]
ACPI Sleep State [S3 (Suspend to R...]
S3 Video Repost [Disabled]
Enables or Disables BIOS ACPI Auto Configuration.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

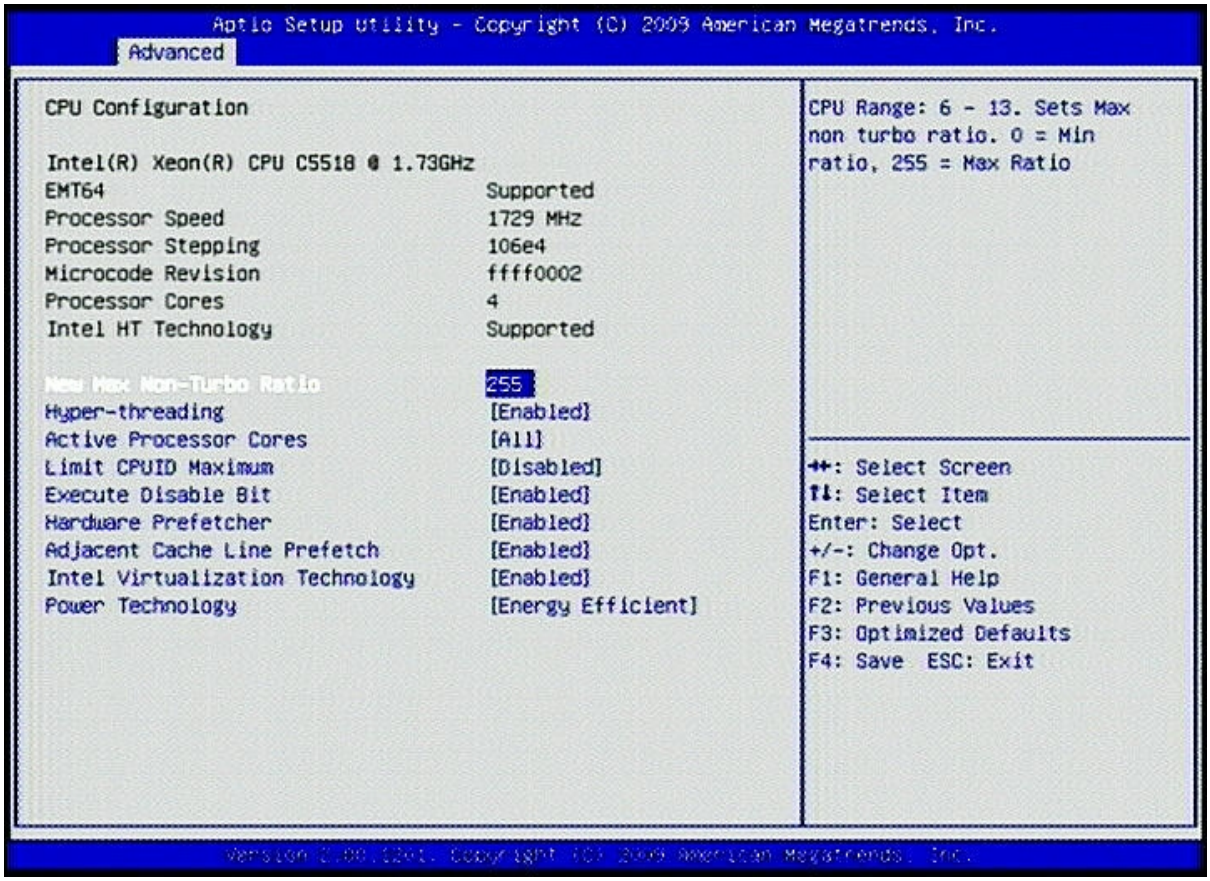
Enable ACPI Auto Configuration
Choices: Enabled, Disabled.

Enable Hiberrnation
Choices: Enabled, Disabled.

ACPI Sleep State
Choices: Suspend Disabled, S1 (CPU Stop Clock), S3 (Suspend to RAM)

S3 Video Report
Choices: Enabled, Disabled.

CPU Configuration
These items show the advanced specifications of your CPU. Read only.


Aptio Setup Utility - Copyright (C) 2009 American Megatrends, Inc.
Advanced
CPU Configuration
Intel(R) Xeon(R) CPU C5518 @ 1.73GHz
EMT64 Supported
Processor Speed 1729 MHz
Processor Stepping 106e4
Microcode Revision ffff0002
Processor Cores 4
Intel HT Technology Supported
New Max Non-Turbo Ratio 255
Hyper-threading [Enabled]
Active Processor Cores [All]
Limit CPUID Maximum [Disabled]
Execute Disable Bit [Enabled]
Hardware Prefetcher [Enabled]
Adjacent Cache Line Prefetch [Enabled]
Intel Virtualization Technology [Enabled]
Power Technology [Energy Efficient]
CPU Range: 6 - 13. Sets Max non turbo ratio. 0 = Min ratio, 255 = Max Ratio
++: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

New Max Non-Turbo Ratio
Choices: 0-255.

Hyper-Threading
Choices: Disabled, Enabled.

Active Processor Cores
Choices: All, 1, 2

Limit CPUID Maximum

Disabled for Windows XP

Choices: Disabled, Enabled.

Execute Disable Bit

Choices: Disabled, Enabled.

Hardware Prefetcher

For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance the specific application.

Choices: Disabled, Enabled.

Adjacent Cache Line Prefetch

For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance the specific application.

Choices: Disabled, Enabled.

Intel Virtualization Technology

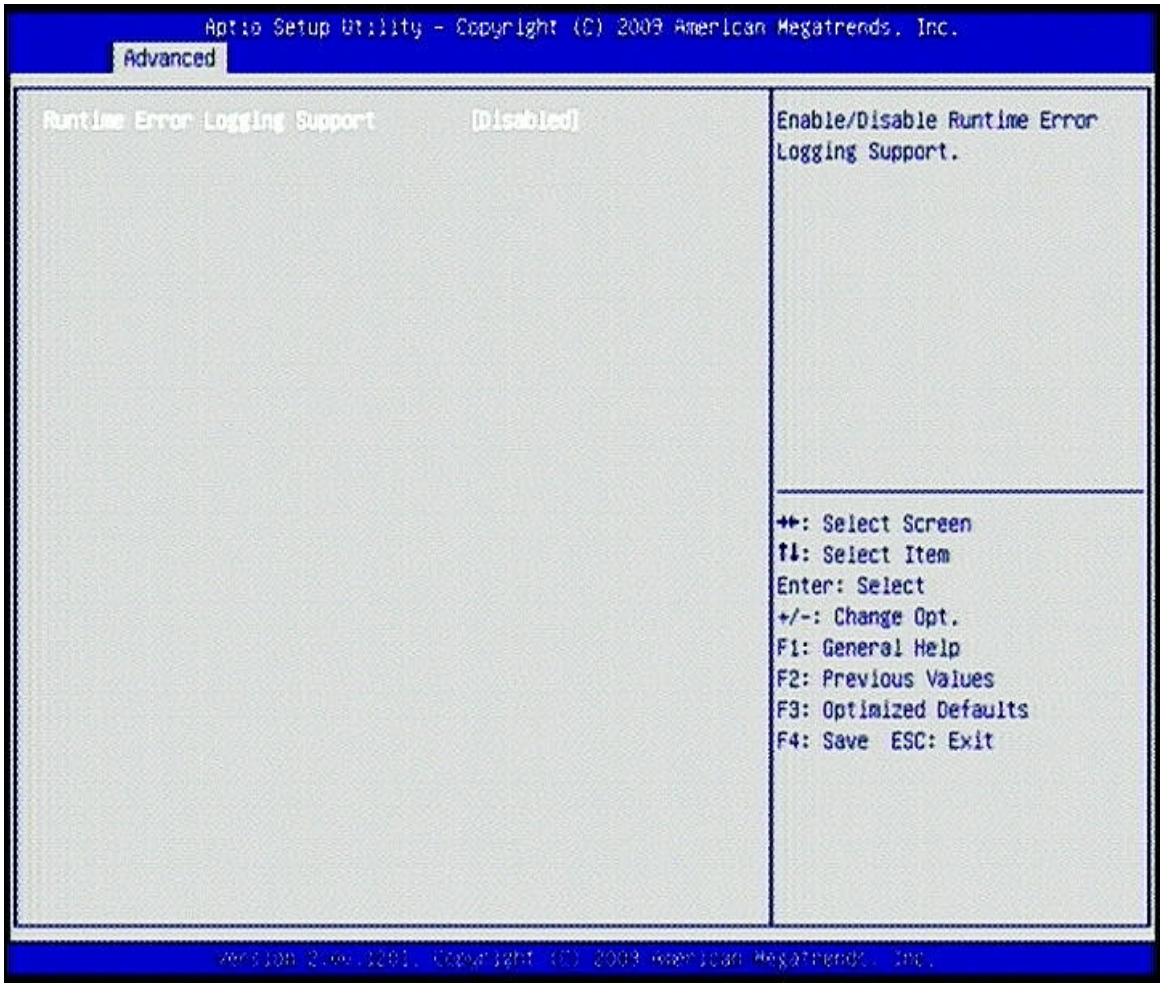
Choices: Disabled, Enabled.

Power Technology

Choices: Disabled, Energy Efficient, Custom

Runtime error Logging

Runtime Error Logging Support Setup Options.

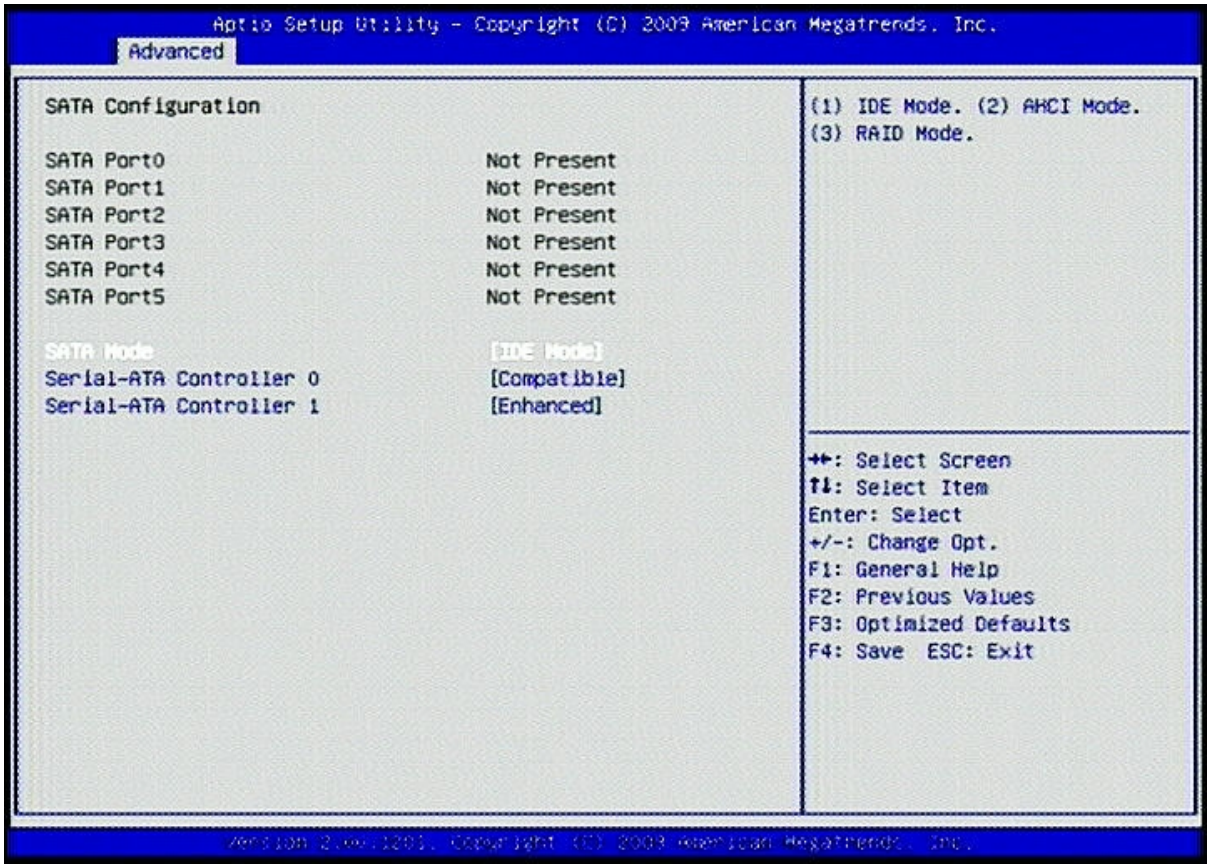


Runtime error Logging Support

Choices: Disabled, Enabled.

SATA Configuration

The SATA Configuration the SATA devices, such as hard disk drive or CD-ROM drive.



SATA Mode

This setting specifies the function of the on-chip SATA controller.

Choices: Disabled, IDE Mode, RAID Mode, AHCI Mode.

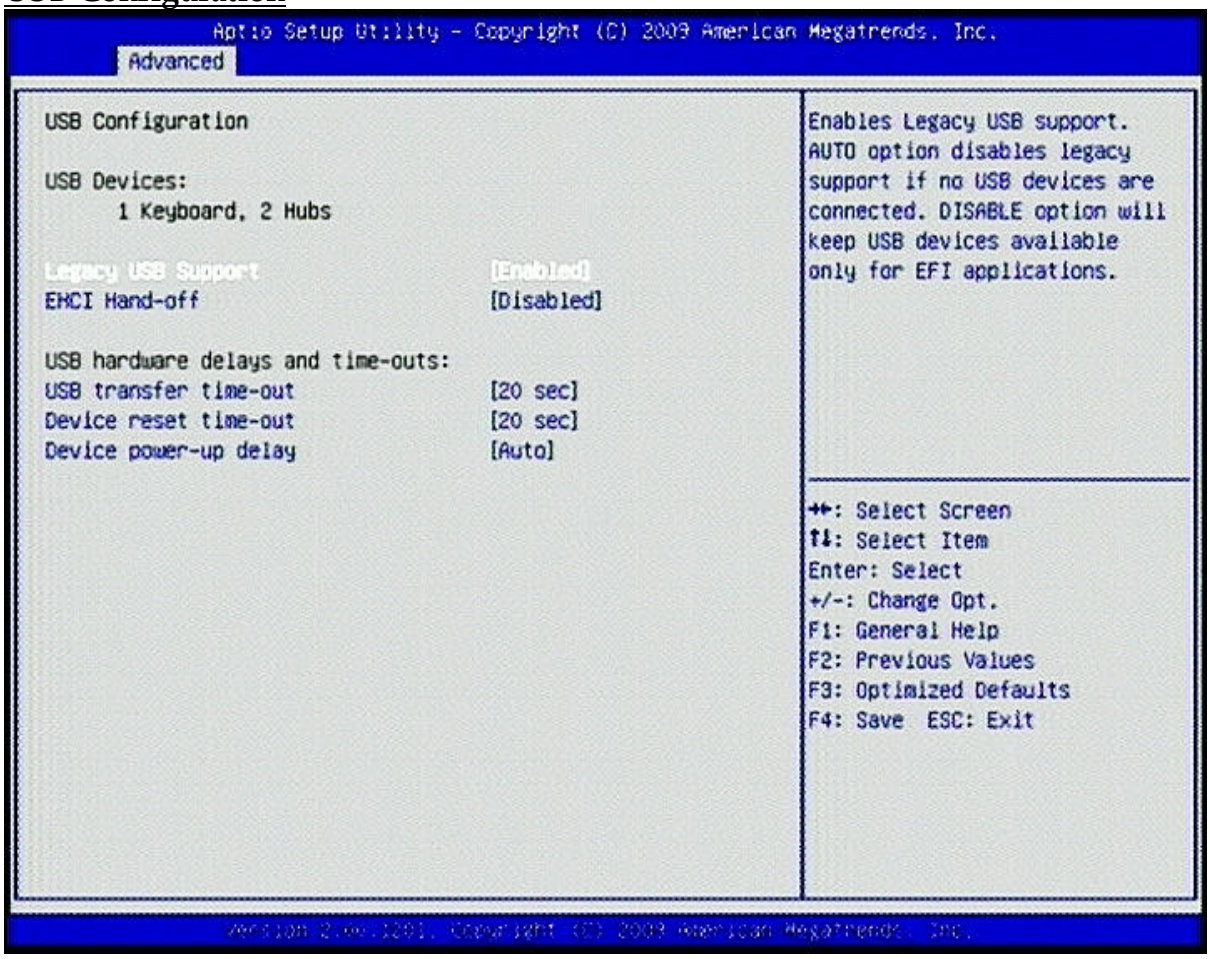
Serial_ATA Controller 0

Choices: Disabled, Compatible, Enabled.

Serial_ATA Controller 1

Choices: Disabled, Compatible, Enabled.

USB Configuration


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
USB Configuration
USB Devices:
1 Keyboard, 2 Hubs
Legacy USB Support [Enabled]
EHCI Hand-off [Disabled]
USB hardware delays and time-outs:
USB transfer time-out [20 sec]
Device reset time-out [20 sec]
Device power-up delay [Auto]
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

Legacy USB Support

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

Choices: Disabled, Enabled, Auto.

EHCI Hand-Off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

Choices: Disabled, Enabled.

USB transfer timeout

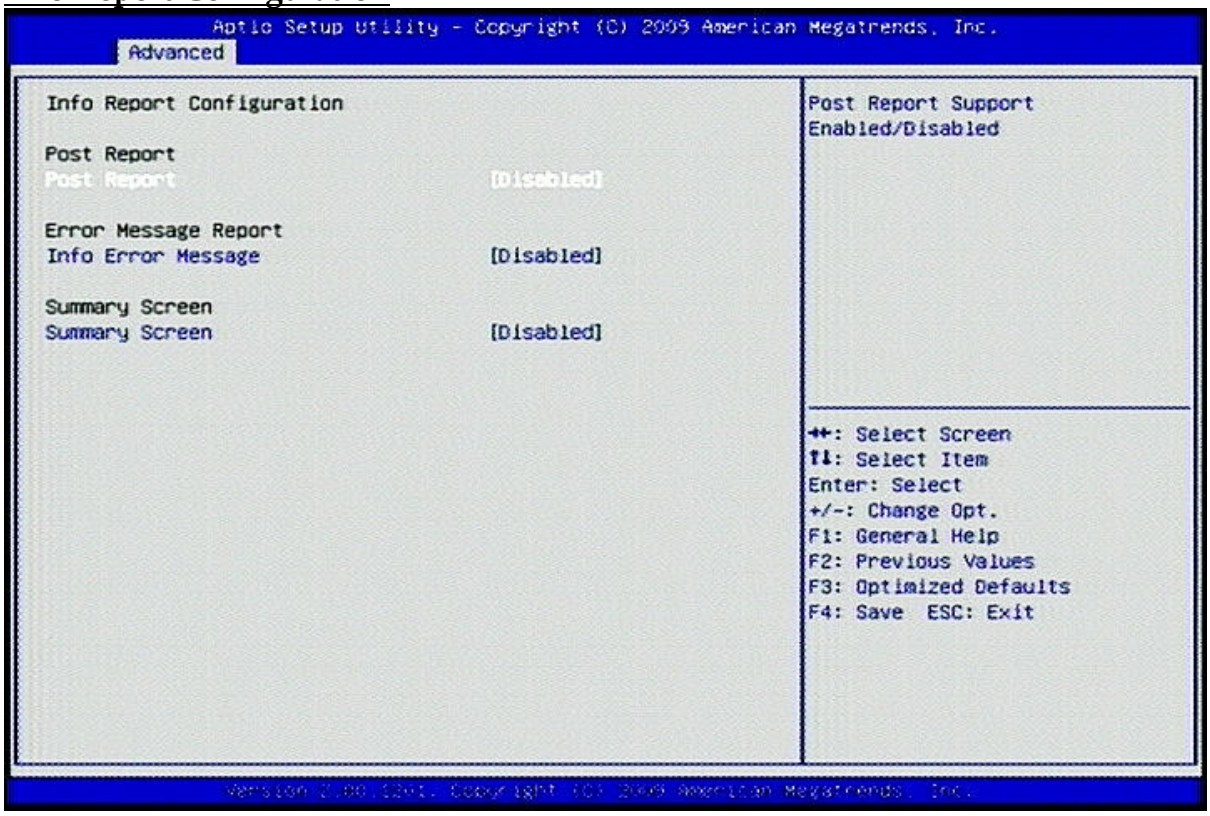
Choices: 1 sec, 5 sec, 10 sec, 20 sec

Device Reset timeout

Choices: 10 sec, 20 sec, 30 sec, 40 sec

Device power-up delay
Choices: Auto, Manual.

Info Report Configuration

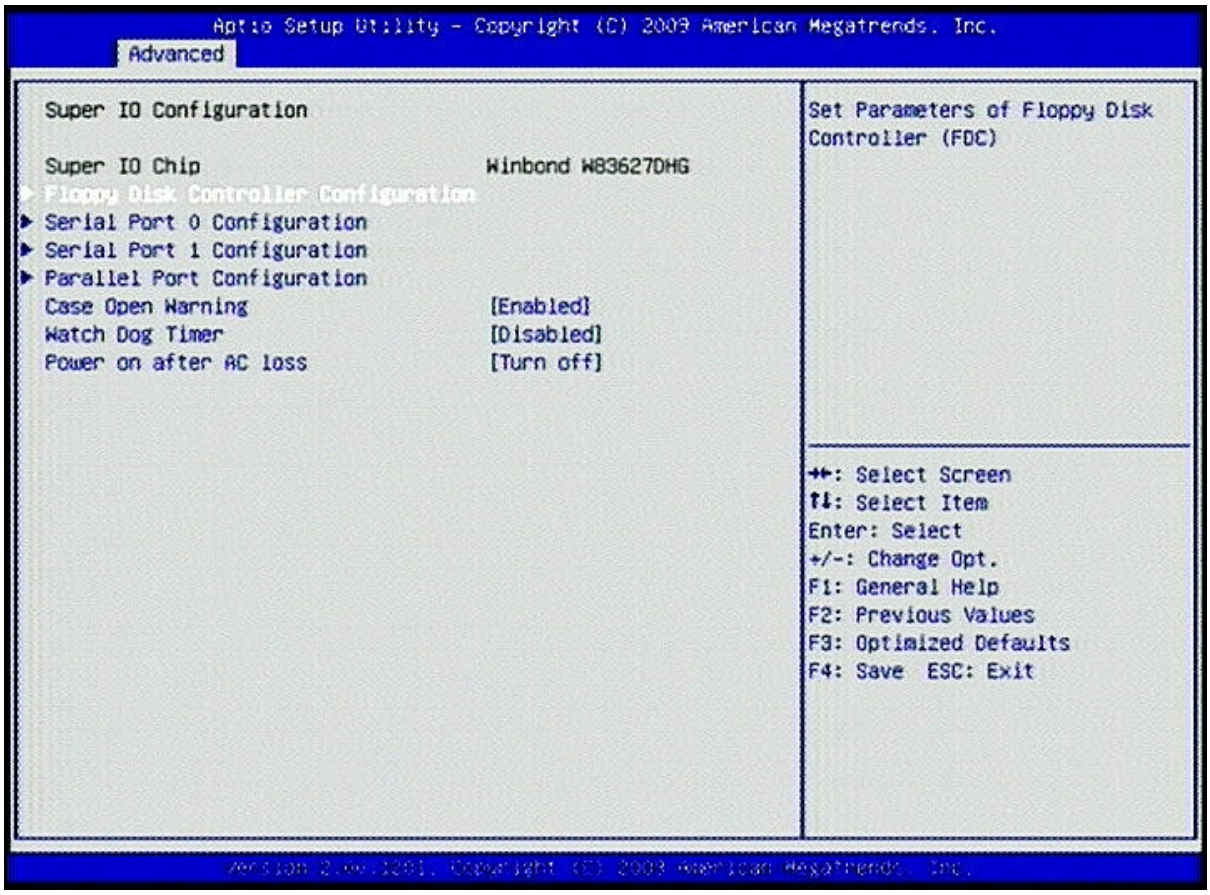


Post Report
Choices: Disabled, Enabled

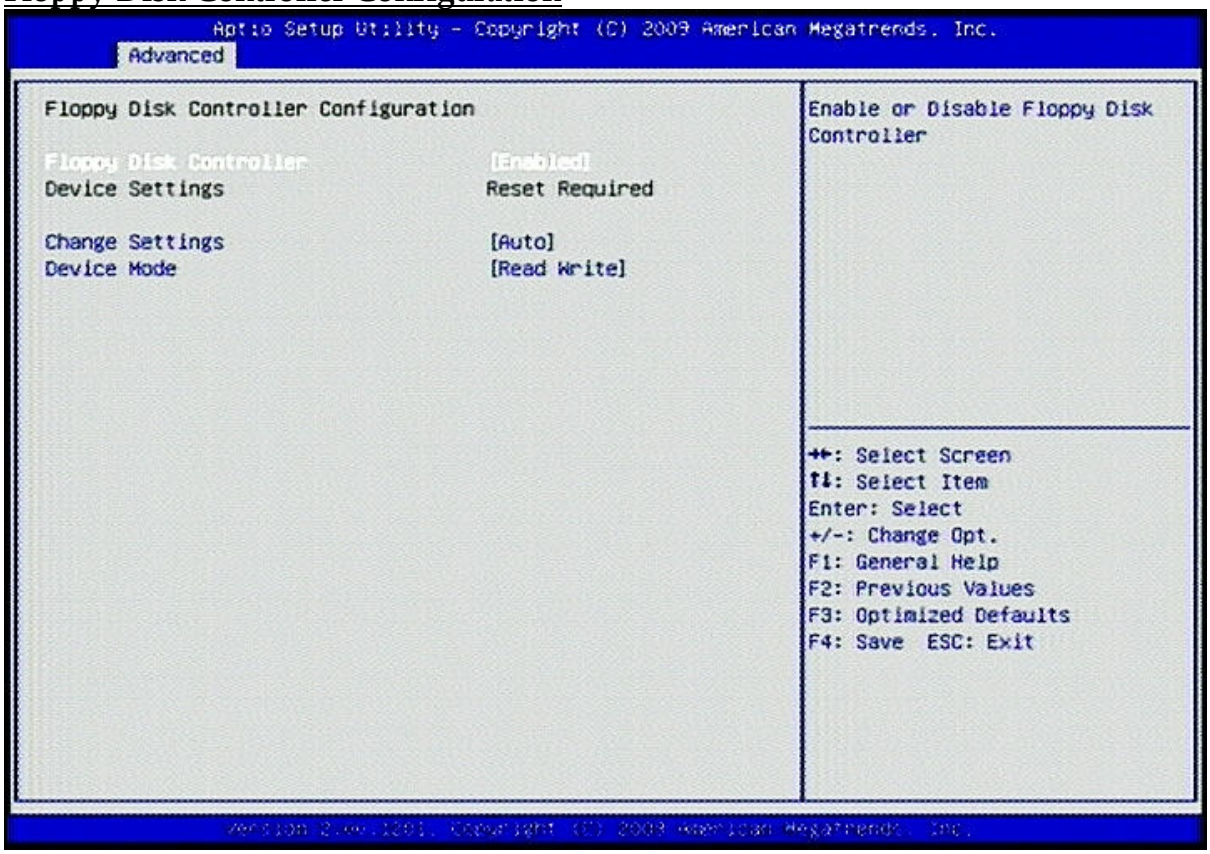
Info Error Message
Choices: Disabled, Enabled

Summary Screen
Choices: Disabled, Enabled

Super IO Configuratoin
List all the option that can be set of Super I/O.
Including Floppy Disk control, Serial Port 0,1 Configuration and Parallel Port configuration,



Floppy Disk Controller Configuration

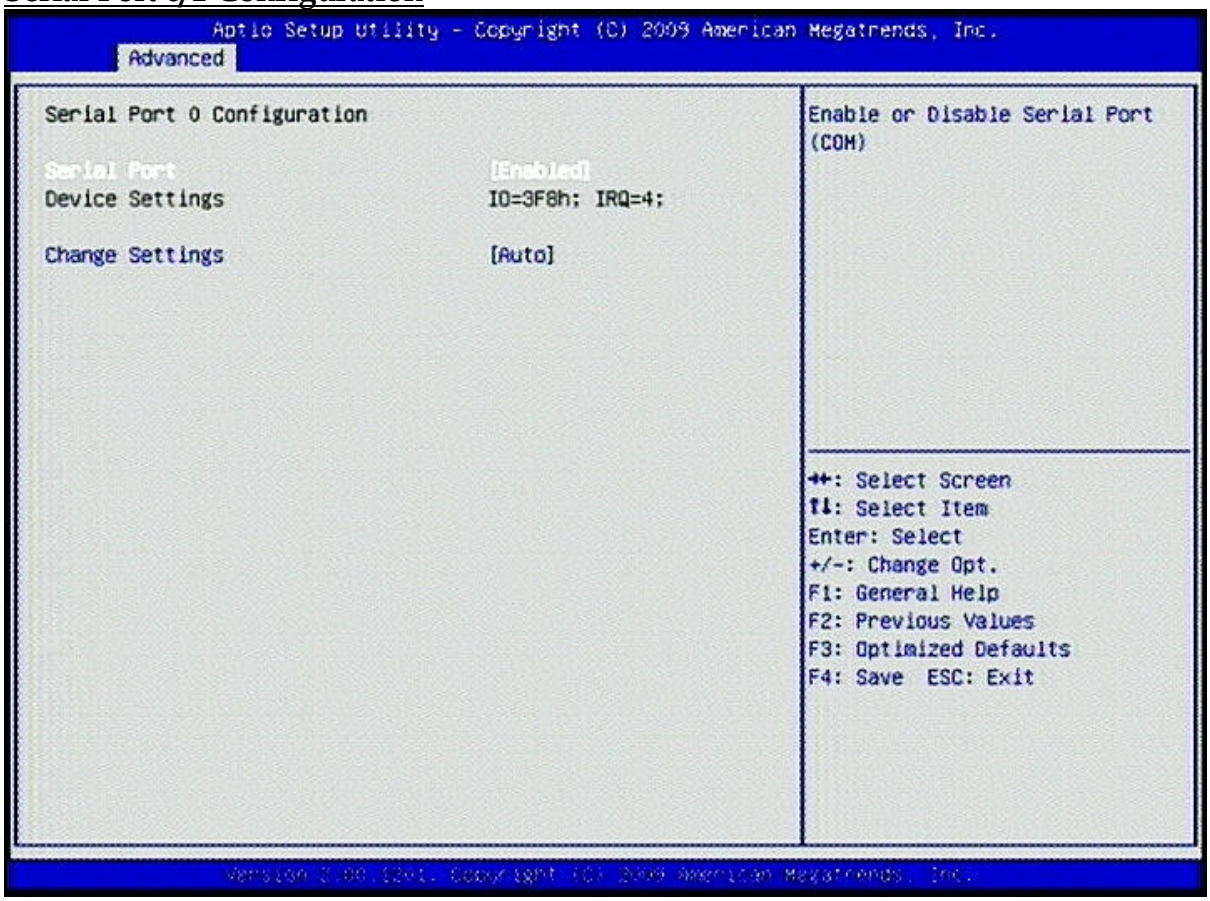


Floppy Disk Controller
Choices: Disabled, Enabled

Change Settings
Choices: Auto, IO=3F0h; IRQ=6, DMA=2;
IO=3F0h; IRQ=3,4,5,6,7,10,11,12, DMA=2, 3;
IO=370h; IRQ=3,4,5,6,7,10,11,12, DMA=2, 3;

Device Mode
Choices: Read Write, Write Protect

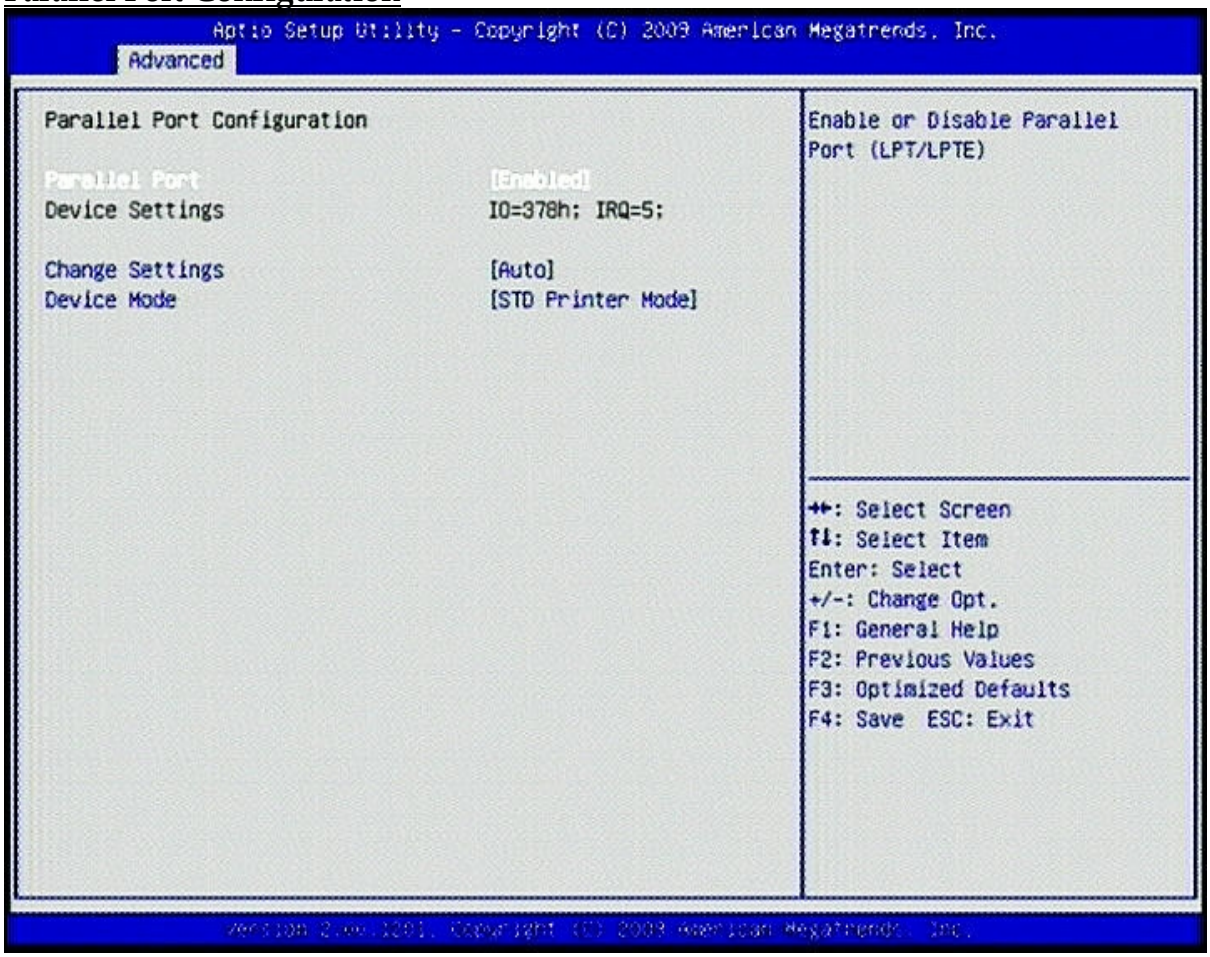
Serial Port 0/1 Configuration



Serial Port
Choices: Disabled, Enabled,

Change Settings
Choices: Auto. IO=3F8h; IRO=4, IO=3F8h; IRO=3,4,5,6,7,10,11,12, IO=2F8h; IRO=3,4,5,6,7,10,11,12, IO=3E8h; IRO=3,4,5,6,7,10,11,12, IO=2E8h; IRO=3,4,5,6,7,10,11,12,

Parallel Port Configuration



Parallel Port
Choices: Disabled, Enabled,

Change Settings
Choices: Auto. IO=378h; IRQ=5, IO=378h; IRO=5,6,7,10,11,12, IO=378h; IRQ=5,6,7,10,11,12, IO=278h; IRQ=5,6,7,10,11,12, IO=38Ch; IRQ=5,6,7,10,11,12,

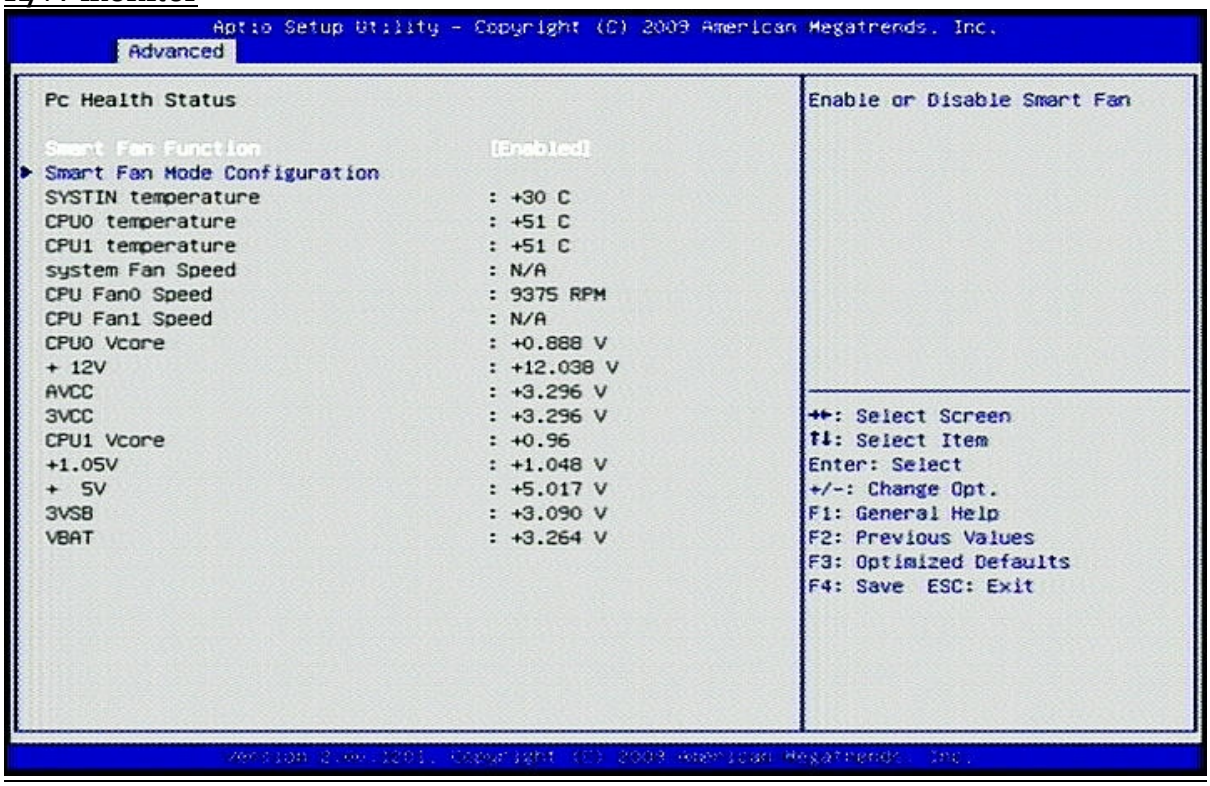
Device Mode
Choices: STD printer mode, SPP mode, EPP-1.9 and SPP mode, EPP-1.7 and SPP mode, ECP mode, ECP and EPP-1.9 mode, ECP and EPP-1.7 mode.

Case Open Warning
Choices: Disabled, Enabled

Watch Dog Timer
Choices: Disabled, Enabled

Power On after AC loss
Choices: Turn off, Turn on

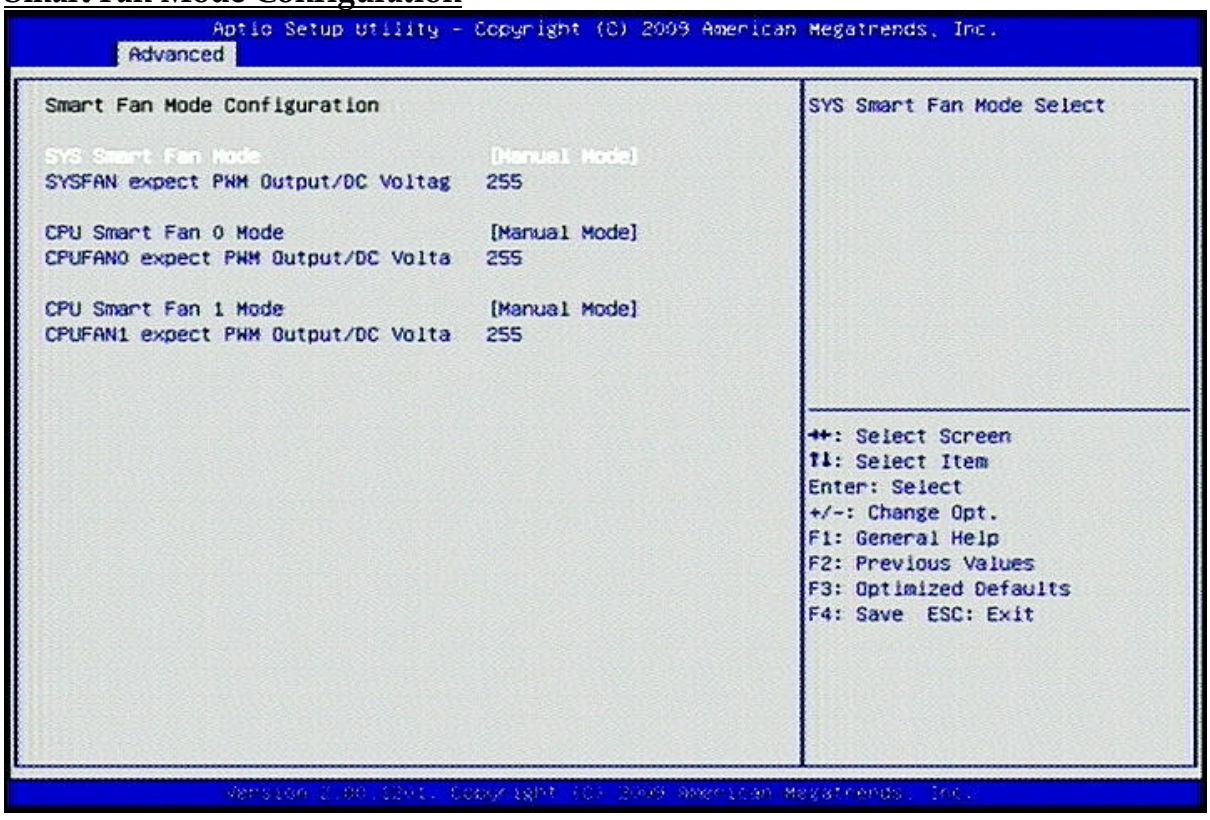
H/W monitor


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Pc Health Status
Smart Fan Function [Enabled]
Smart Fan Mode Configuration
SYSTIN temperature : +30 C
CPU0 temperature : +51 C
CPU1 temperature : +51 C
system Fan Speed : N/A
CPU Fan0 Speed : 9375 RPM
CPU Fan1 Speed : N/A
CPU0 Vcore : +0.888 V
+ 12V : +12.038 V
AVCC : +3.296 V
3VCC : +3.296 V
CPU1 Vcore : +0.96
+1.05V : +1.048 V
+ 5V : +5.017 V
3VSB : +3.090 V
VBAT : +3.264 V
Enable or Disable Smart Fan
↔: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

Smart Fan Function

Choices: Disabled, Enabled

Smart Fan Mode Configuration


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Smart Fan Mode Configuration
SYS Smart Fan Mode [Manual Mode]
SYSFAN expect PWM Output/DC Voltag 255
CPU Smart Fan 0 Mode [Manual Mode]
CPUFAN0 expect PWM Output/DC Volta 255
CPU Smart Fan 1 Mode [Manual Mode]
CPUFAN1 expect PWM Output/DC Volta 255
SYS Smart Fan Mode Select
↔: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

System Smart Fan Mode
Choices: Manual Mode, Thermal Cruise Mode, Fan Speed Cruise Mode.

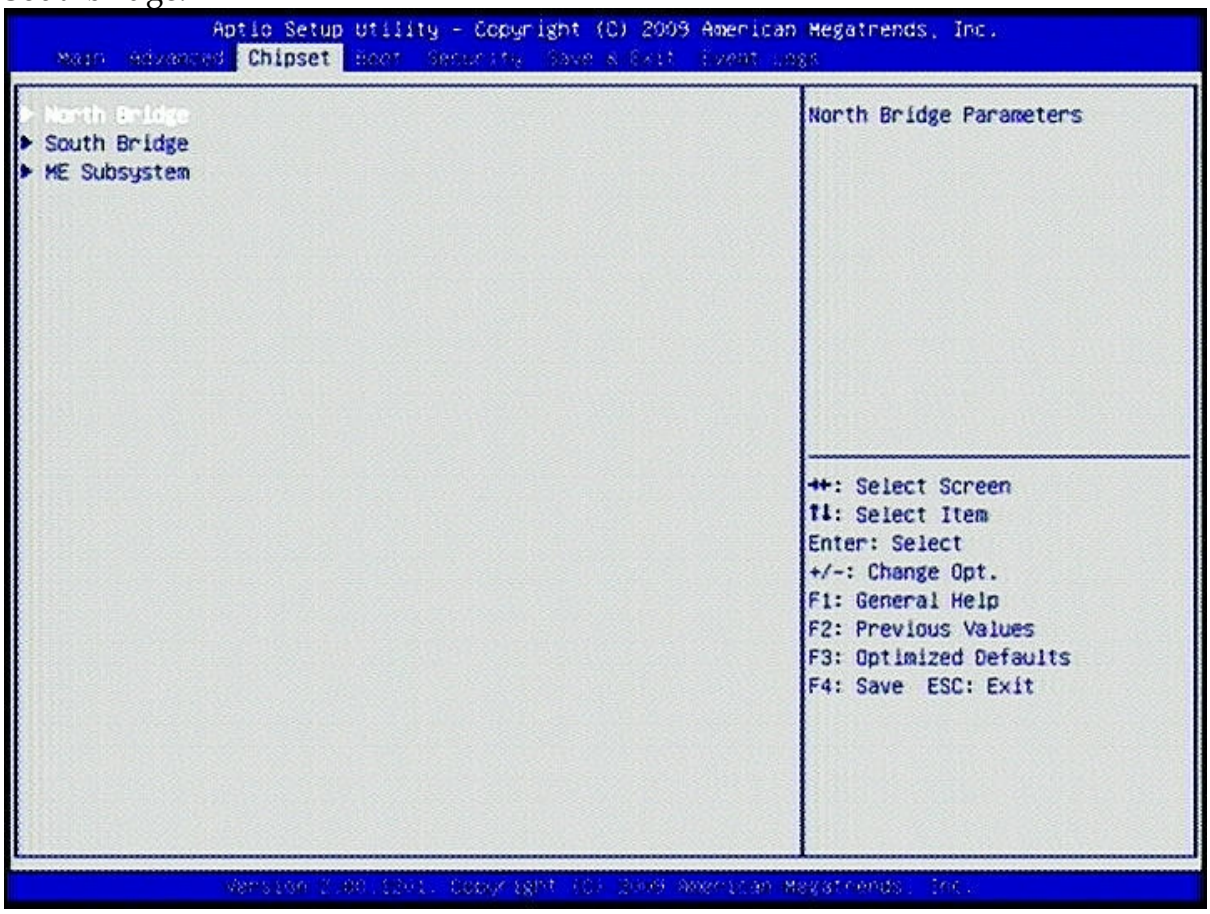
System expect PWM Output/DC Volta
Choices: 0-255.

CPU Smart Fan 0/1 Mode
Choices: Manual Mode, Thermal Cruise Mode, Fan Speed Cruise Mode, Smart Fan III Mode.

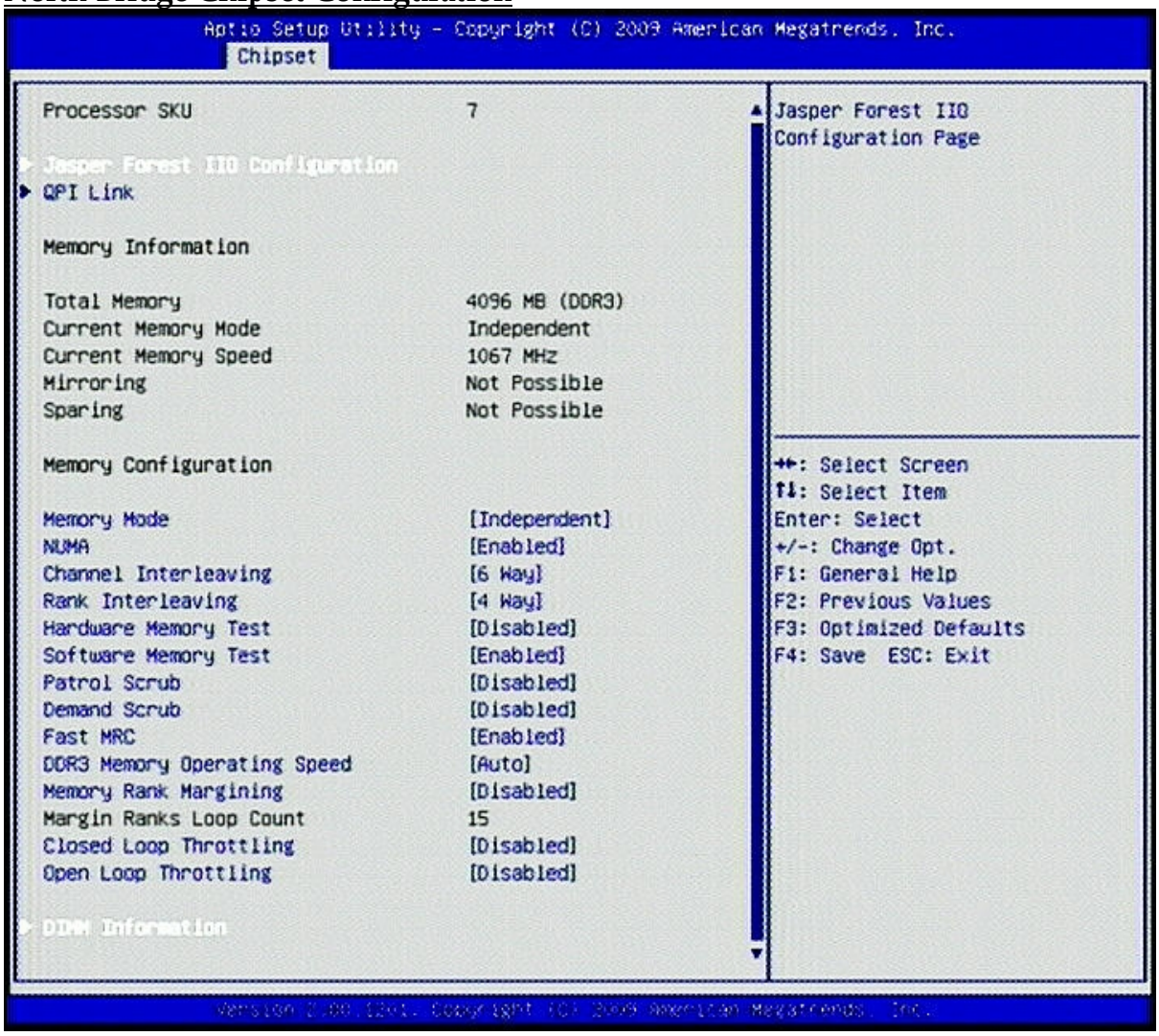
CPUFAN0/1 expect PWM Output/DC Volta
Choices: 0-255.

4.4 Chipset

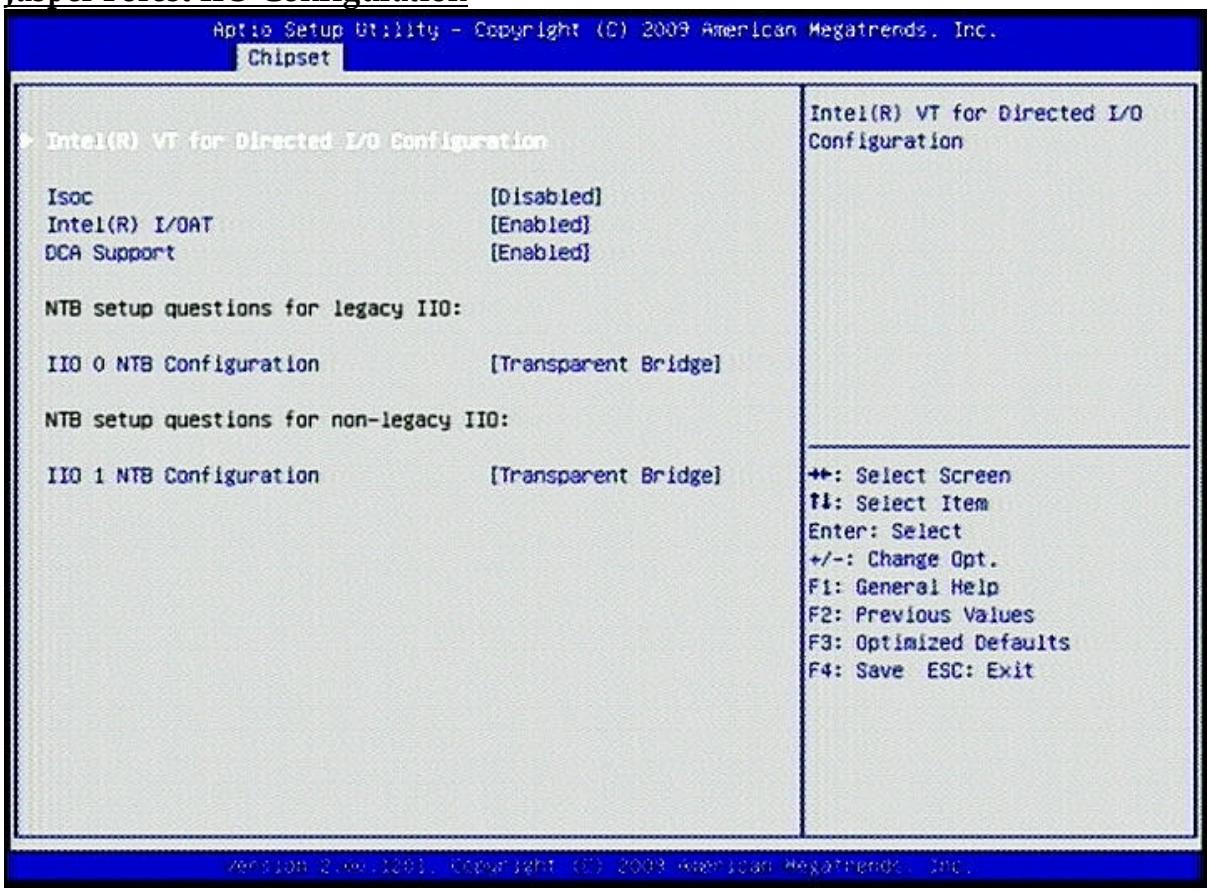
This menu controls the advanced features of the onboard Northbridge and Southbridge.



North Bridge Chipset Configuration



Jasper Forest IIO Configuration


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Chipset
Intel(R) VT for Directed I/O Configuration
Isoc [Disabled]
Intel(R) I/OAT [Enabled]
DCA Support [Enabled]
NTB setup questions for legacy IIO:
IIO 0 NTB Configuration [Transparent Bridge]
NTB setup questions for non-legacy IIO:
IIO 1 NTB Configuration [Transparent Bridge]
Intel(R) VT for Directed I/O Configuration
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

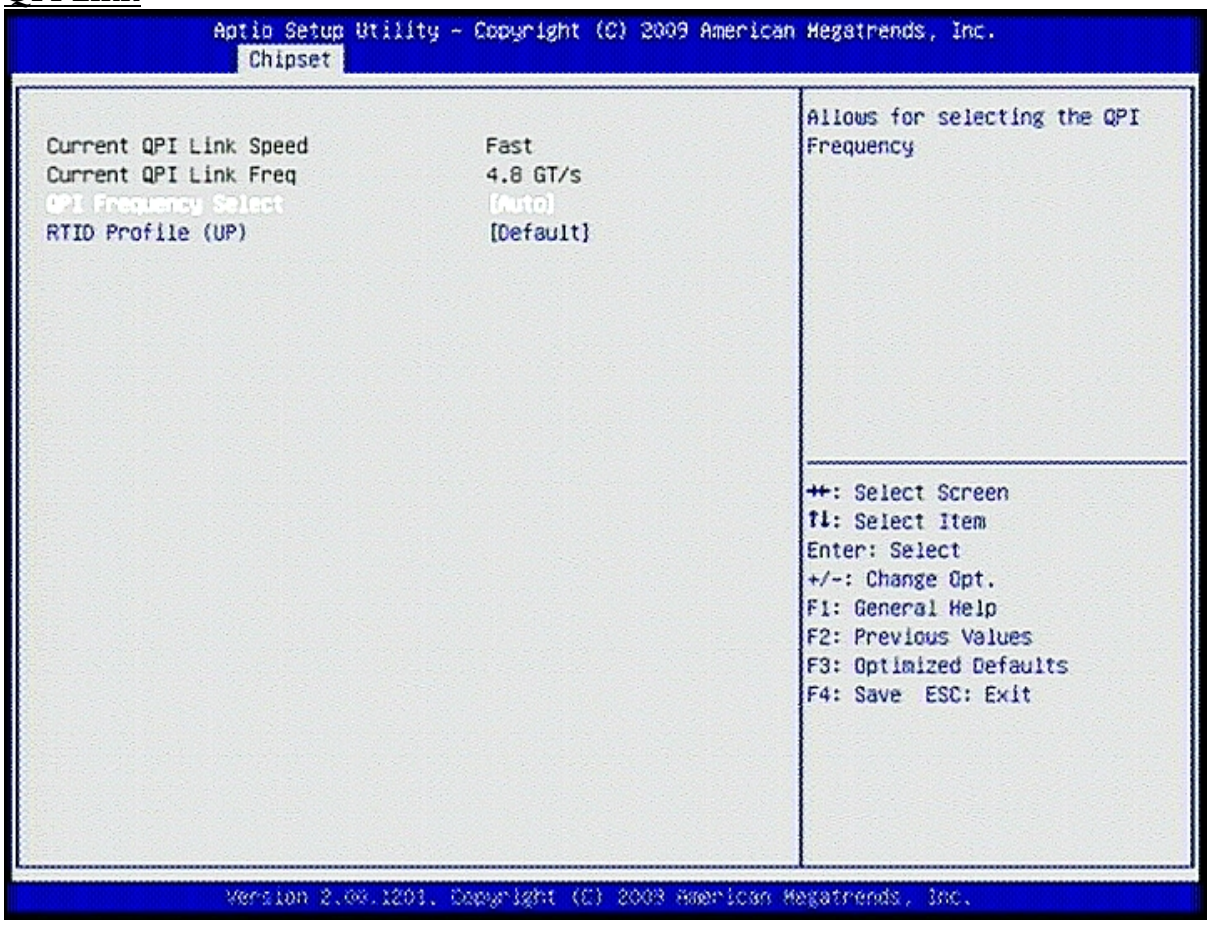
Isoc
Choices: Disabled, Auto, Enabled.

Intel(R) I/OAT
Choices: Disabled, Enabled.

DCA Support
Choices: Disabled, Enabled.

IIO0/1 NTB Configuration
Choices: Transparent Bridge, NTB to NTB, NTB to RP.

QPI Link



QPI Frequency Select
Choices: Auto, 5.866GT/s, 4.8GT/s, 4.270 GT/s, Disable Fast mode.

RTID Profile(UP)
Choices: Default, UP IO-Centric.

Memory Mode
Choices: Independent, Mirroring, Lock Step, Sparing.

NUMA
Choices: Disabled, Enabled,

Channel Interleaving
Choices: Auto, 6 Way, 4 Way, 3 Way, 2 Way, 1 Way.

Rank Interleaving
Choices: Auto, 4 Way, 2 Way, 1 Way.

Hardware Memory Test
Choices: Disabled, Enabled.

Software Memory Test
Choices: Disabled, Enabled.

Patrol Scrub
Choices: Disabled, Enabled.

Demand Scrub
Choices: Disabled, Enabled.

Fast MRC
Choices: Disabled, Enabled.

DDR3 Memory Operating Speed
Choices: Auto, 1333MHz, 1067MHz, 800MHz.

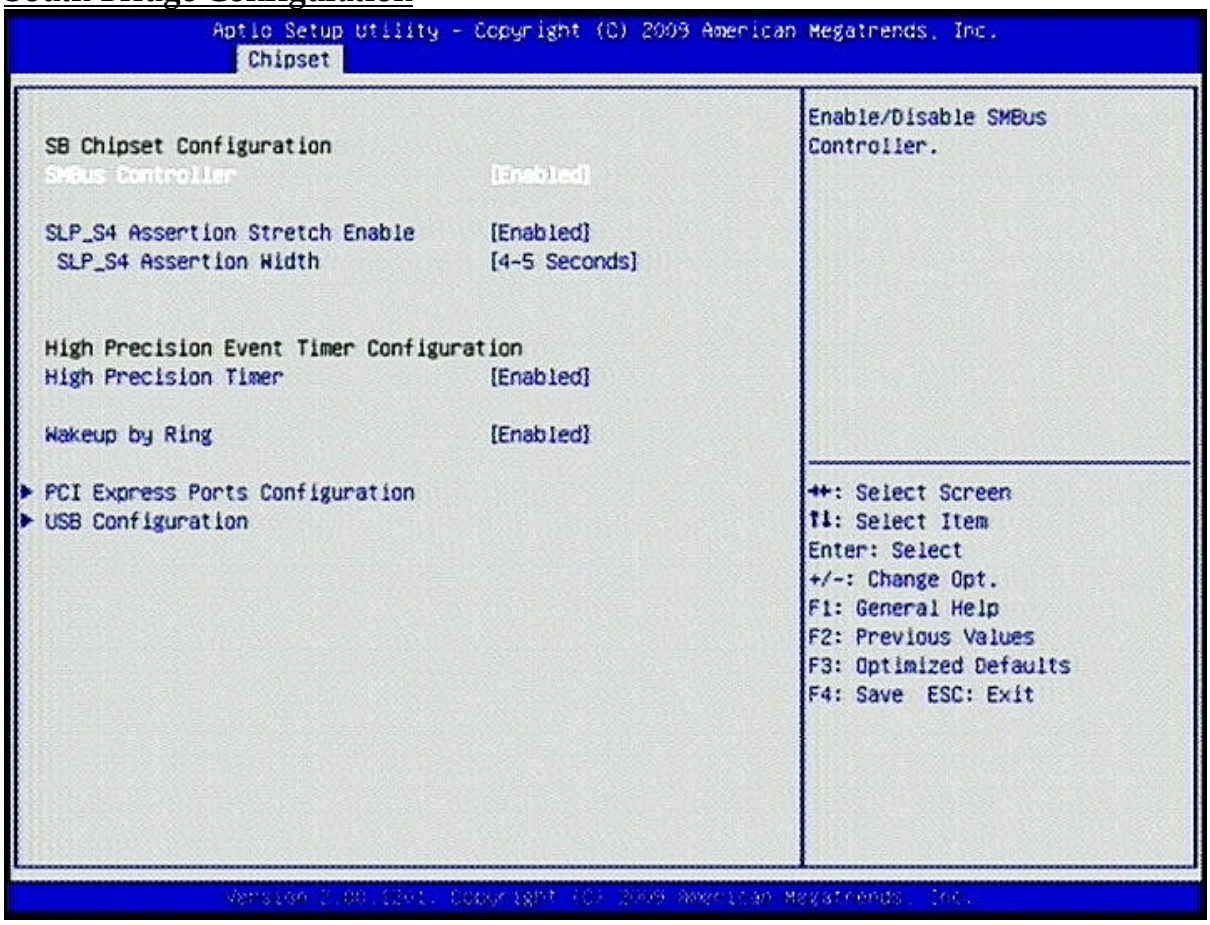
Memory Rank Margining
Choices: Auto, 1333MHz, 1067MHz, 800MHz.

Closed Loop Throttling
Choices: Disabled, Enabled.

Open Loop Throttling
Choices: Disabled, Enabled.

DIMM Information
Display DIMM presence and size information.

South Bridge Configuration



SMBus Controller
Choices: Disabled, Enabled,

SLP_S4 Assertion Stretch Enable
Choices: Disabled, Enabled,

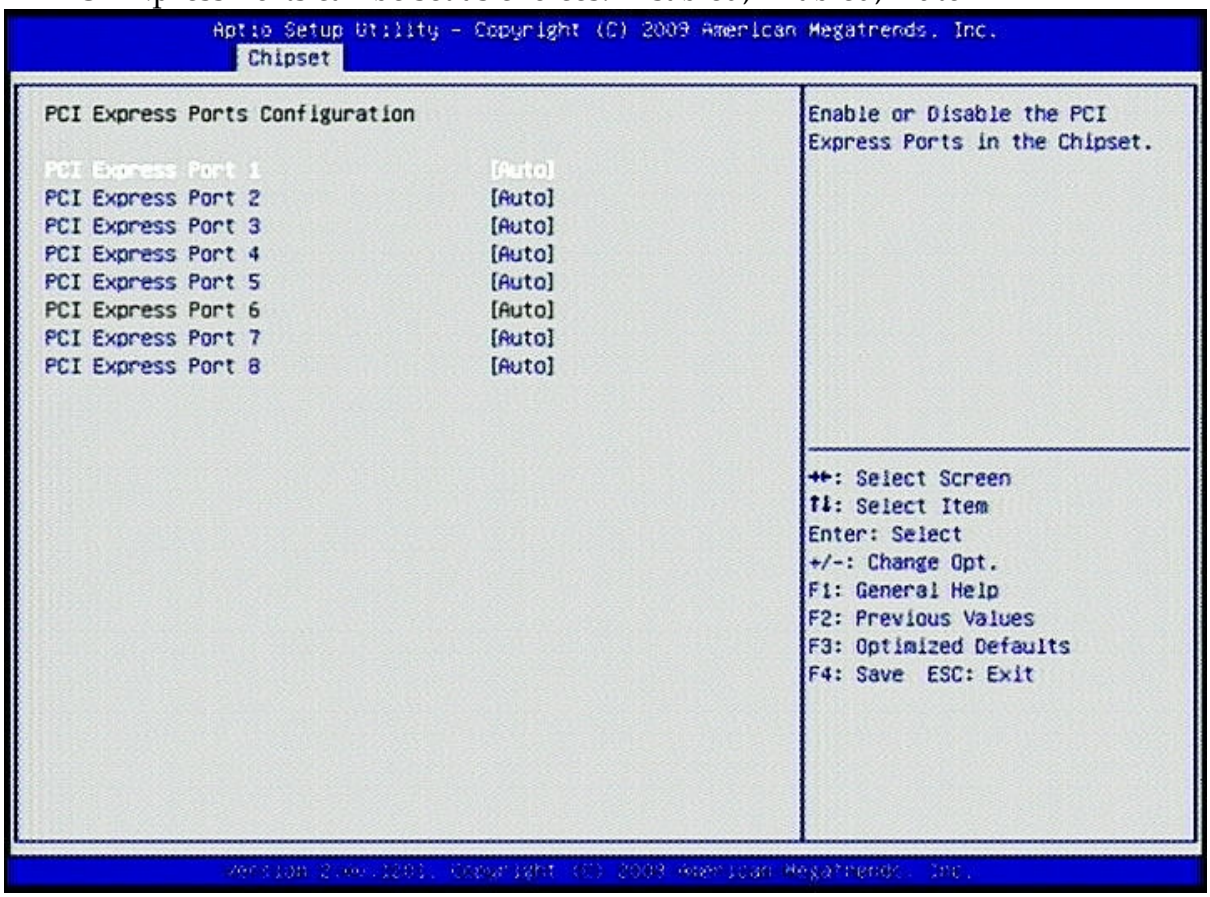
SLP_S4 Assertion Width
Choices: 1-2, 2-3. 3-4, 4-5 seconds

High Precision timer
Choices: Disabled, Enabled,

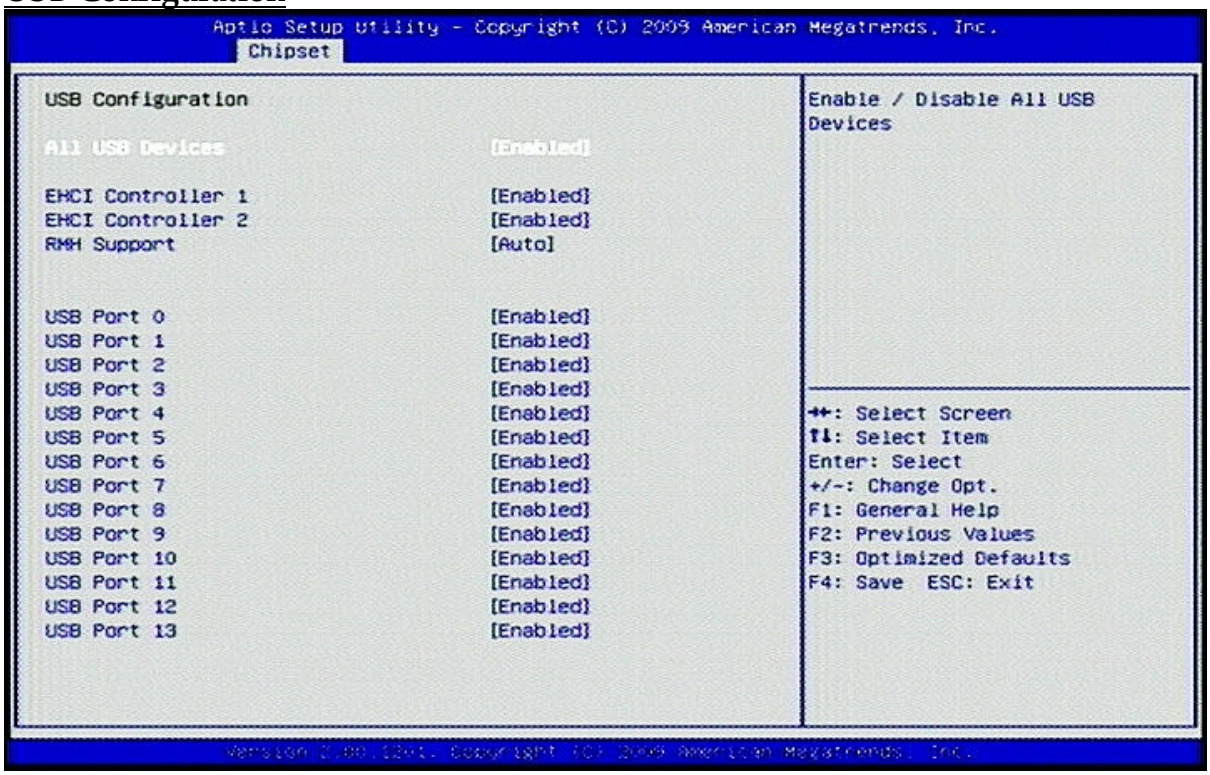
Wakeup by Ring
Choices: Disabled, Enabled,

PCI Express Ports Configuration

All PCI Express Ports can be set as choices: Disabled, Enabled, Auto


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Chipset
PCI Express Ports Configuration
PCI Express Port 1 [Auto]
PCI Express Port 2 [Auto]
PCI Express Port 3 [Auto]
PCI Express Port 4 [Auto]
PCI Express Port 5 [Auto]
PCI Express Port 6 [Auto]
PCI Express Port 7 [Auto]
PCI Express Port 8 [Auto]
Enable or Disable the PCI Express Ports in the Chipset.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

USB Configuration



ALL USB Devices
Choices: Disabled, Enabled

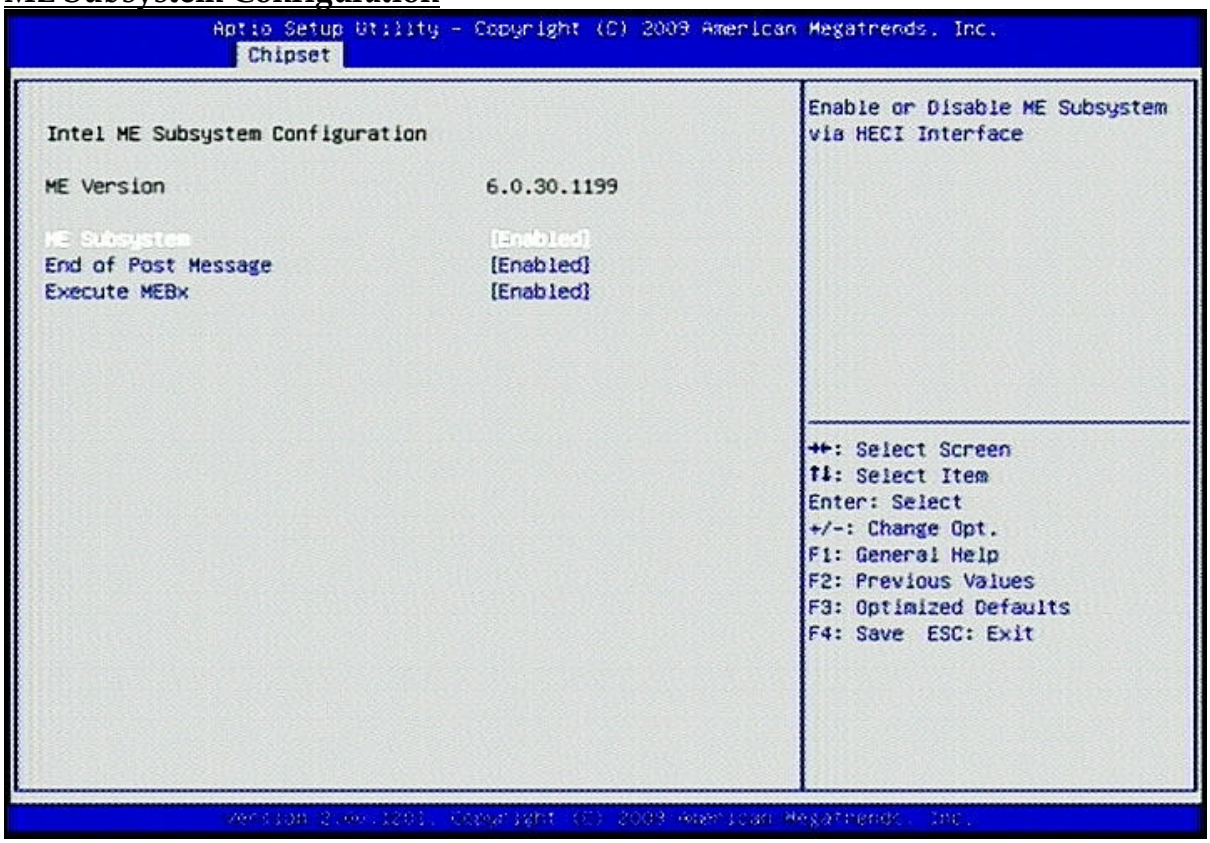
EHCI Controller 1
Choices: Disabled, Enabled

EHCI Controller 2
Choices: Disabled, Enabled

RHM Support
Choices: Disabled, Enabled, Auto

USB Port 0/1/2/3/4/5/6/7/8/9/10/11/12/13
Choices: Disabled, Enabled

ME Subsystem Configuration



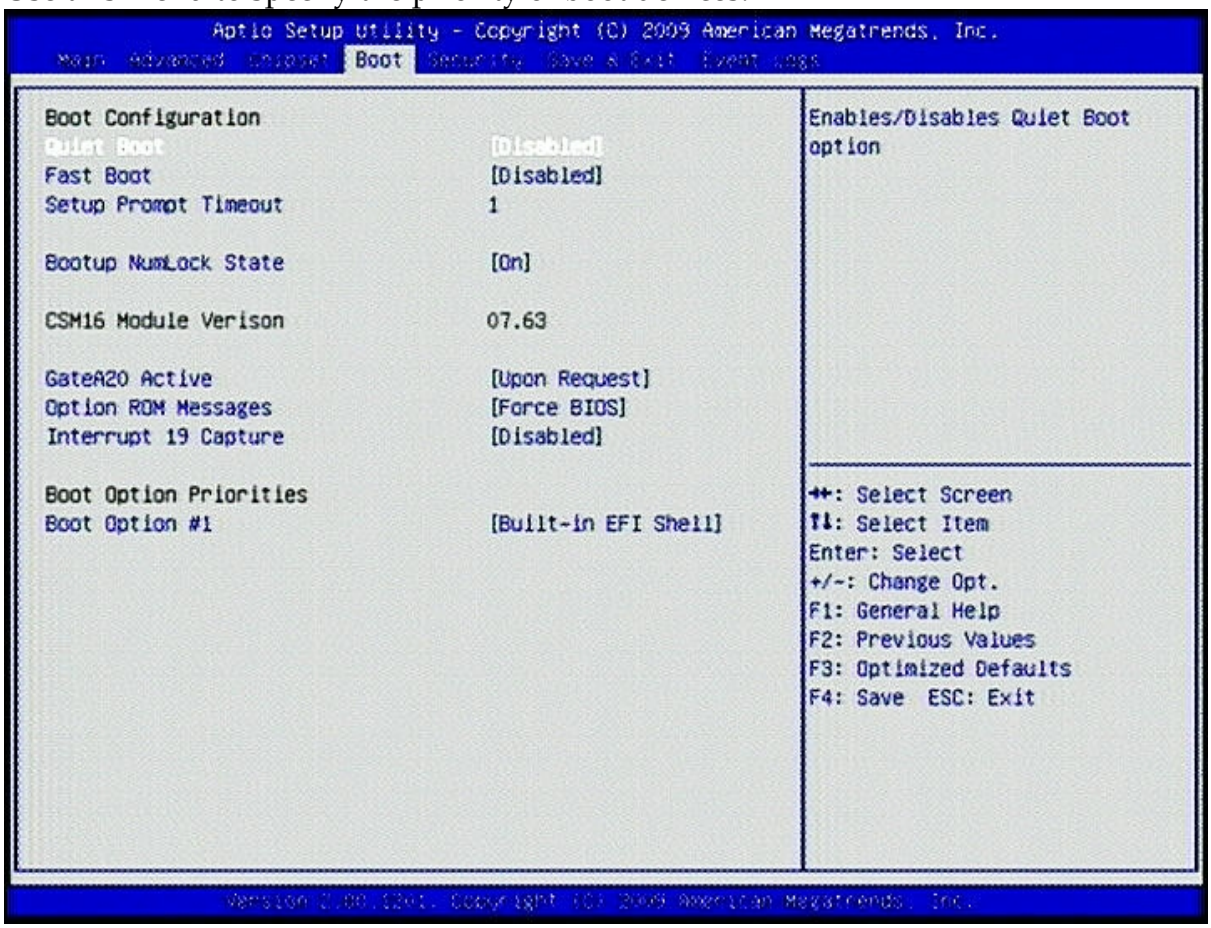
ME Subsystem
Choices: Enabled, Disabled.

End of Post Message
Choices: Enabled, Disabled.

Execute MEBx
Choices: Enabled, Disabled.

4.5 Boot

Use this menu to specify the priority of boot devices.



Quiet Boot

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.

When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

Choices: Disabled, Enabled.

Fast Boot

Enabling this setting will cause the BIOS power-on self test routine to skip some of its tests during boot up for faster system boot.

Choices: Disabled, Enabled.

Setup Prompt Timeout
Choices: 1-65535

Bootup Num-Lock State

This setting is to set the Num Lock status when the system is powered on. Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

Choices: On, Off.

GateA20 Active
Choices: Upon Request, Always

Option ROM Messages
This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

Choices: Force BIOS, Keep Current.

Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.

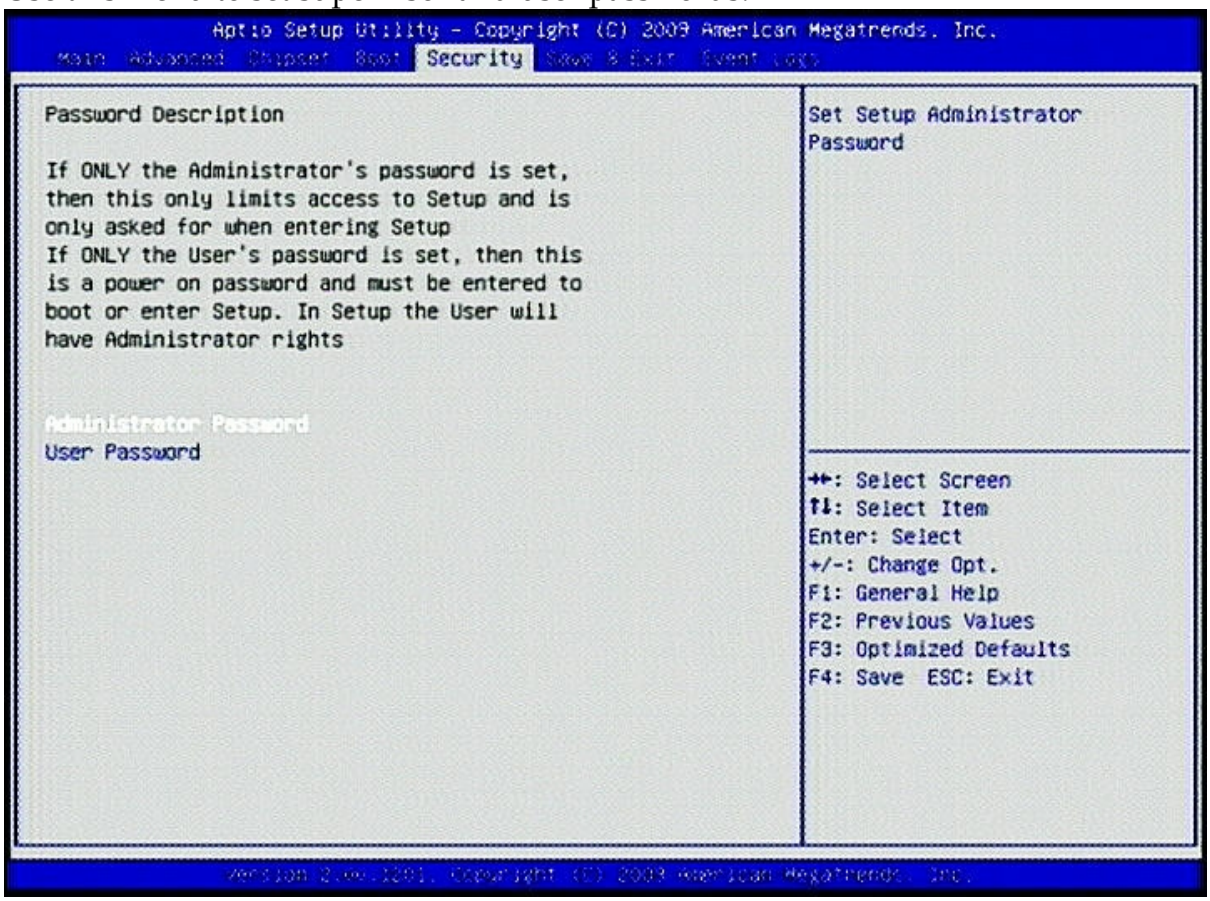
When disabled, the ROM BIOS of these host adaptors will not be able to "cap ture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

Choices: Disabled, Enabled.

Boot Option # 1
Choices: Built-in EFI Shell, Disable, Other Devices.

4.6 Security

Use this menu to set supervisor and user passwords.


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Security
Password Description
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights
Administrator Password
User Password
Set Setup Administrator Password
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

Administrator Password

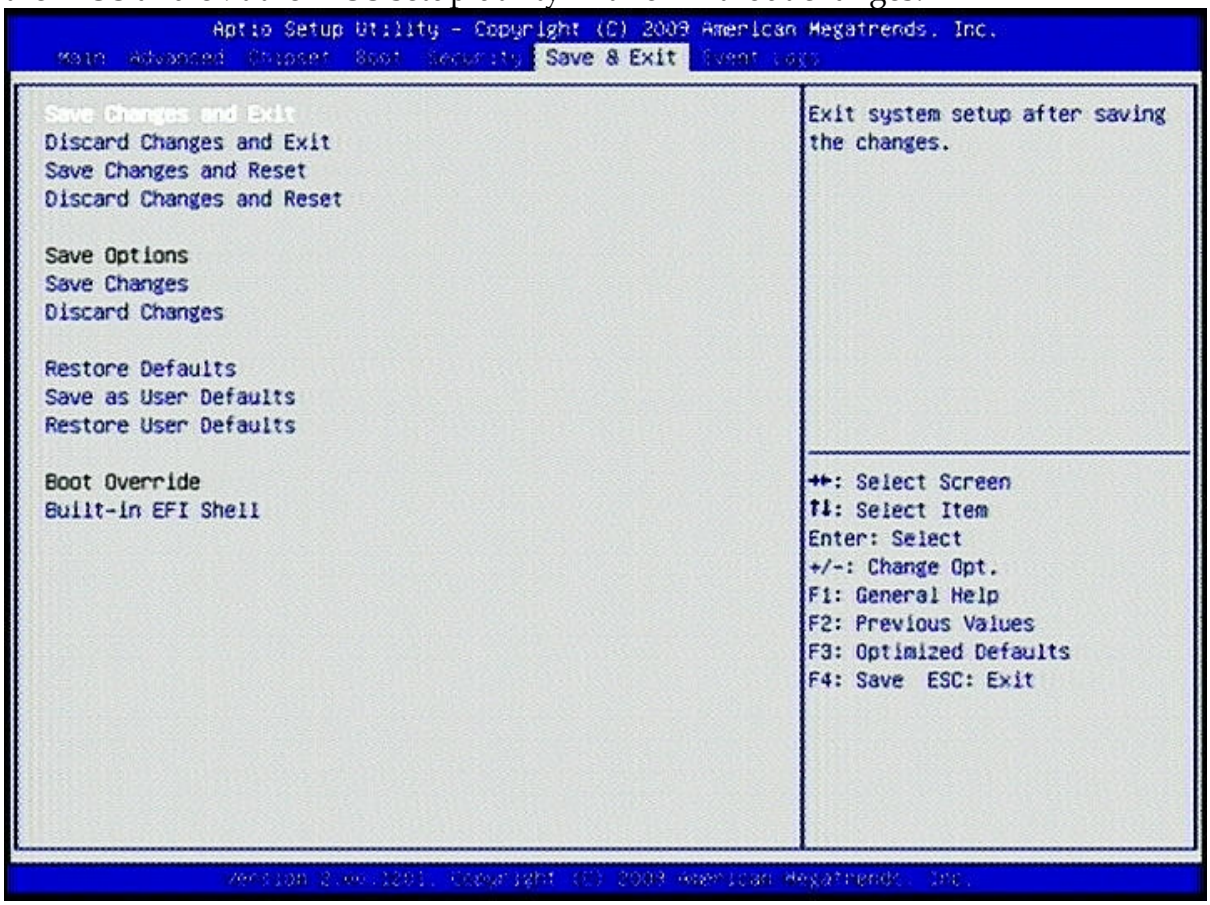
Administrator Password controls access to the BIOS Setup utility. These settings allow you to set or change the supervisor password.

User Password

User Password controls access to the system at boot. These settings allow you to set or change the user password.

4.7 Save & Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.



Save Changes and Exit
Exit System Setup and save your changes to CMOS. Pressing <Enter> on this item asks for confirmation: Save changes to CMOS and exit the Setup Utility.

Discard Changes and Exit
Abandon all changes and exit the Setup Utility.

Save Changes and Reset
Exit System Setup and save your changes to CMOS then reboot.

Discard Changes and Reset
Abandon all changes and exit the Setup Utility then reboot

Save Changes
Save all changes and continue with the Setup Utility.

Discard Changes

Abandon all changes and continue with the Setup Utility.

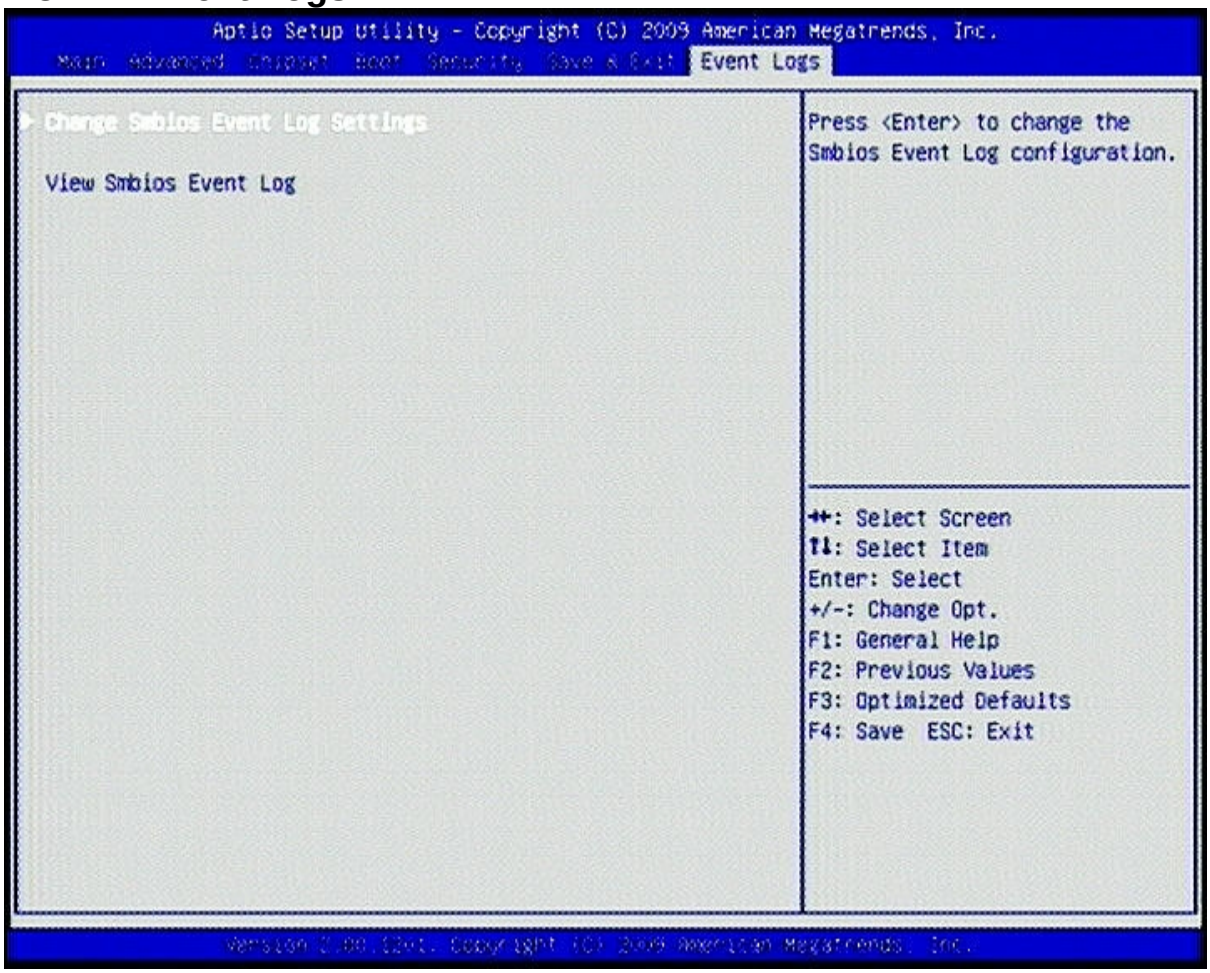
Restore Defaults
Use this menu to load the default values set by the SBC manufacturer specifically for optimal performance of the SBC.

Save as User Defaults
Save all changes and considers as User's default.

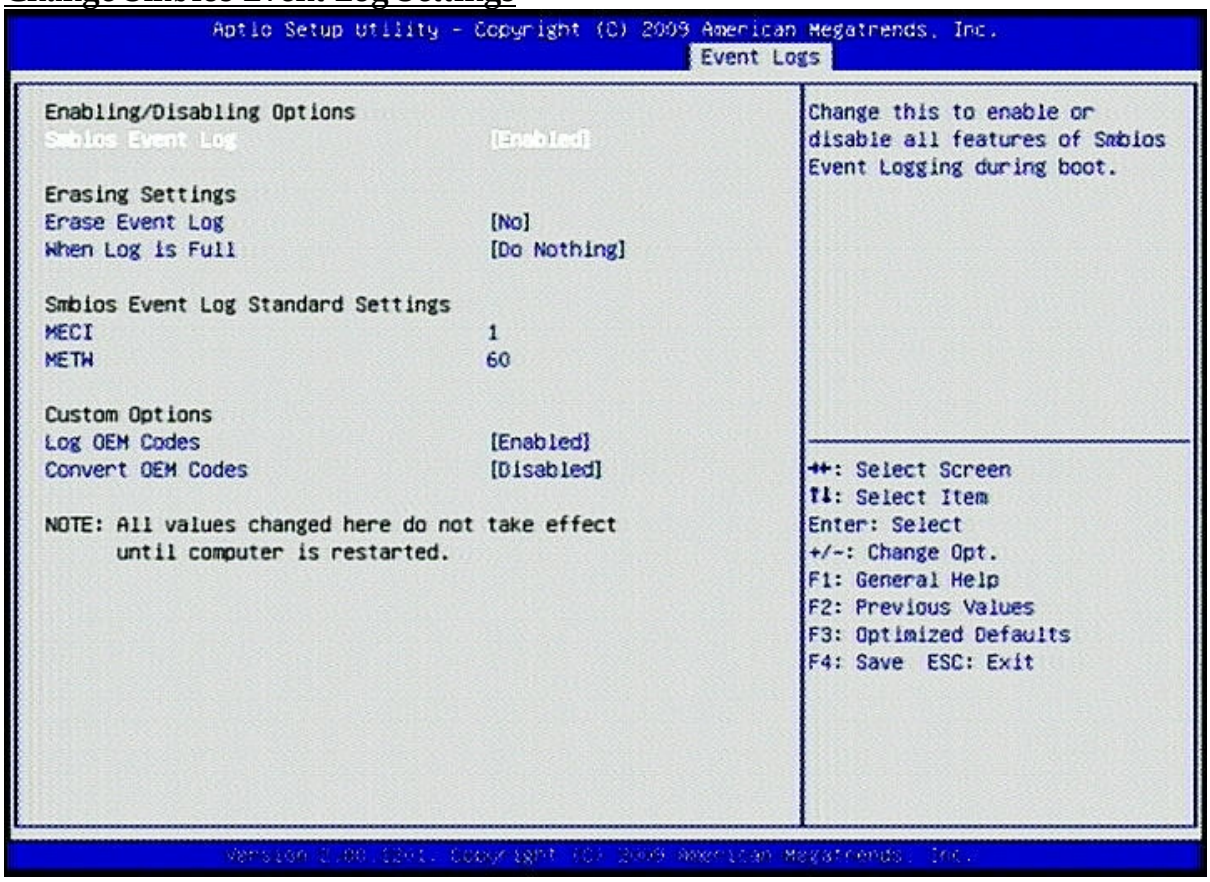
Restore User Default
Restore the setting according to User's default

Built-in EFI Shell
To enter the Built-in EFI shell for further modification such as upgrade BIOS.

4.8 Event Logs


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Event Logs
Change Smbios Event Log Settings
View Smbios Event Log
Press <Enter> to change the Smbios Event Log configuration.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

Change Smbios Event Log Settings


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Event Logs
Enabling/Disabling Options
Smbios Event Log [Enabled]
Erasing Settings
Erase Event Log [No]
When Log is Full [Do Nothing]
Smbios Event Log Standard Settings
MECI 1
METW 60
Custom Options
Log OEM Codes [Enabled]
Convert OEM Codes [Disabled]
NOTE: All values changed here do not take effect until computer is restarted.
Change this to enable or disable all features of Smbios Event Logging during boot.
↔: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

Smbios Event Log
Choices: Enabled, Disabled.

Erase Event Log
Choices: No, Yes, Next reset, Yes, Every reset.

When Log is Full
Choices: Do Nothing, Erase Immediately.

MECI
Choices: 1-255.

METW
Choices: 0-99.

Log OEM Codes
Choices: Enabled, Disabled.

Convert OEM Codes
Choices: Enabled, Disabled.

View Smbios Event Log
View smbios event log.

Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get ROBO-8120VG2R running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting

Unlike other Single board computer, ROBO-8120VG2R supports ATX only. Therefore, there is no other setting that really needs to be set up. However, there are only two connectors that must be connected—PWR2 (24 pins Power Connector) and PWR1.

Serial ATA Hard Disk Setting for IDE/RAID/AHCI

Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time; there are total four connectors, SATA1~4 port. The installation of Serial ATA is simpler and easier than IDE, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to operate IDE, RAID (0/1) and AHCI application for system, please follow up setting guide in BIOS programming (Table 5-1).

Detect sequence: SATA1 → SATA2 → SATA3 → SATA4
SATA1 -- Primary IDE Master
SATA2 -- Secondary IDE Master
SATA3 -- Primary IDE Slave
SATA4 -- Secondary IDE Slave

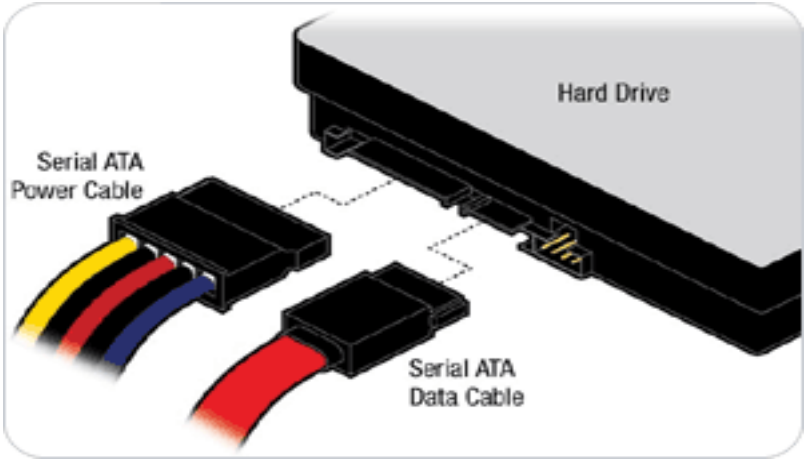


Table. 5-1 SATA Mode setting guide

5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. CPU, CPU Fan, 240-pin DDR3 SDRAM, keyboard, mouse, floppy drive, SATA hard disk, DVI-I connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with ROBO-8120VG2R, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to "**Restore Defaults** ", press "Enter" and "Y" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Auto Detect Hard Disks

In the BIOS => Standard CMOS setup menu, pick up any one from Primary/Secondary Master/Slave IDE ports, and press "Enter". Setup the selected IDE port and its access mode to "Auto". This will force system to automatically pick up the IDE devices that are being connected each time system boots up.

Improper disable operation

There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the COM1/ COM2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

Disable COM1 serial port to release IRQ #4
Disable COM2 serial port to release IRQ #3

Etc…

A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	**System Timer**
IRQ #1	**Keyboard Event**
IRQ #2	**Usable IRQ**
IRQ #3	**COM2**
IRQ #4	**COM1**
IRQ #5	**Usable IRQ**
IRQ #6	**Diskette Event**
IRQ #7	**Usable IRQ**
IRQ #8	**Real-Time Clock**
IRQ #9	**Usable IRQ**
IRQ #10	**Usable IRQ**
IRQ #11	**Usable IRQ**
IRQ #12	**IBM Mouse Event**
IRQ #13	**Coprocessor Error**
IRQ #14	**Hard Disk Event**
IRQ #15	**Usable IRQ**

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FAQ

Installation Problem

Question:I forget my password of system BIOS, what am I supposed to do?

Answer: You can simply short 2-3 pins on JP3 to clean your password.

Note:
Please visit our technical web site at
http://www.portwell.com.tw
For additional technical information, which is not covered in this manual, you can mail to tsd@mail.portwell.com.tw or you can also send mail to our sales, they wull be very delighted to forward them to us.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used.

Memory Area	Size	Device Description
Memory Area	*Size*	*Description*
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-06D6	25K	DOS
06D7-15E8	60K	Program Area
15E9-9E7F	546K	【Available】
First Meg -- Conventional memory end at 634K --		
9EC0-9FFF	5K	Extended BIOS Area
9E80-9EBF	1K	Unused
A000-AFFF	64K	VGA Graphics
B000-B7FF	32K	Unused
B800-BFFF	32K	VGA Text
C000-C7FF	32K	Video ROM
C800-EFFF	160K	Unused
F000-FFFF	64K	System ROM
HMA	64K	First 64K Extended
Memory Area	*Size*	*Description*
0000-003F	1K	Interrupt Area

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	【Unassigned】	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	【Unassigned】	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	【Unassigned】	Usable IRQ
IRQ 8	System ROM	Real-Time Clock

IRQ 9	【Unassigned】	Usable IRQ
IRQ 10	【Unassigned】	Usable IRQ
IRQ 11	【Unassigned】	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	【Unassigned】	Usable IRQ